### COE 561, Term 111 Digital System Design and Synthesis Course Project

The list of course projects proposed for this term are as shown below. In each project, the main objective of the project and the expected team members are specified. Each student must select a project according to the deadlines specified below.

#### **1.** Evaluation of Defect-Tolerant Multi-Crosspoint Architecture for Nanoscale Crossbar Based Logic Circuits [2 Students]

Nanoscale crossbars are manufactured using bottom-up fabrication processes which are projected to have higher defect densities in comparison to conventional CMOS fabrication. Thus, defect-tolerant design techniques will be a necessity in future nanoscale crossbar based logic circuits. In this project, students will implement and evaluate a defect-tolerant architecture that adds redundancy in the rows and columns of a nanoscale crossbar and provides built-in immunity to stuck-open crosspoint defects. The students will perform simulations using benchmark circuits to compare area and defect tolerance of the redundancy-based defect-tolerant crossbar architecture against monomorphism-based defect avoidance technique.

#### 2. Differential Evolution Based State Assignment for Area Optimization [2 Students]

State assignment (SA) for Finite State Machine (FSM) is one of the main optimization problems in the synthesis of sequential circuits. The SA of an FSM determines the complexity of its combinational circuit and thus area, delay, testability and power dissipation of the implementation.

Differential Evolution (PSO) is an evolutionary algorithm that has been shown to be effective on a large range of classic optimization problems. It has been shown that DE is more accurate than several other optimization methods including genetic algorithms, simulated annealing and evolutionary programming. It iterates over three main steps: mutation, recombination and selection.

In this project, the students are to use the DE algorithm to derive state assignments that optimize the area of a sequential circuit.

Task	Deadline
Project selection	Saturday, Oct. 29
Project Plan	Saturday, Nov. 19
Progress Report	Saturday, Dec. 10
Final Report & Project Demonstration	Saturday, Dec. 31

## **Project Deadlines:**

Each student group is expected to submit a project plan describing the project tasks, the time planned for each task, and the team members' role in each task. Each group is also required to submit a progress report describing briefly the progress made so far in the project against planned work, difficulties faced, results obtained so far and the tasks to be performed in the next period. At the end of the project, each group is required to submit a professional report showing the details of all the work performed and demonstrate their project to me.

# **Project Evaluation Criteria:**

Task	Mark
Project Plan	5%
Progress Report	5%
Project Accomplishments vs. Requirements	60%
Final Report Documentation & Organization	30%