

COE 561, Term 101
Digital System Design and Synthesis
Course Project

The list of course projects proposed for this term are as shown below. In each project, the main objective of the project and the expected team members are specified. Each student must select a project according to the deadlines specified below.

1. Two-Level Logic Synthesis for Soft Error Masking [2 Students]

Due to current technology scaling trends circuit reliability has become more susceptible to radiation-induced transient faults (soft errors). As logic circuits move to higher operating frequencies, lower voltage levels, and smaller noise margins, it is projected that the soft error rates in logic circuits will become unacceptable even for mainstream commercial applications. In this project, students will develop and implement a two-level logic synthesis scheme to maximize soft error masking. Soft error fault tolerance will be evaluated based on simulation.

2. Multi-Level Logic Synthesis for Soft Error Masking [2 Students]

Due to current technology scaling trends circuit reliability has become more susceptible to radiation-induced transient faults (soft errors). As logic circuits move to higher operating frequencies, lower voltage levels, and smaller noise margins, it is projected that the soft error rates in logic circuits will become unacceptable even for mainstream commercial applications. In this project, students will investigate the effect of multi-logic synthesis transformation on soft error masking. This includes single-cube extraction, multiple-cube extraction and fast extraction. Based on the results, students will develop a method for maximizing soft error masking based on multi-level logic synthesis. Soft error fault tolerance will be evaluated based on simulation.

3. Implementation of Signal Probability Evaluation and Resynthesis for Multi-level Circuits [2 Students]

In this project, students will use simulation based technique to compute signal probabilities for all signals in a multi-level circuit. Then, sub-circuits will be selected according to either number of levels or number of inputs or signal probabilities and will be re-synthesized using developed approaches to maximize soft-error masking and the re-synthesized circuit is merged back with the original circuit.

4. Particle Swarm Optimization (PSO) Based State Assignment for Area, Power and Testability [3 Students]

State assignment (SA) for Finite State Machine (FSM) is one of the main optimization problems in the synthesis of sequential circuits. The SA of an FSM determines the complexity of its combinational circuit and thus area, delay, testability and power dissipation of the implementation.

Particle swarm optimization (PSO) is a computational method that optimizes a problem by iteratively trying to improve a candidate solution with regard to a given measure of quality. PSO optimizes a problem by having a population of candidate solutions, particles, and moving these particles around in the search-space according to simple mathematical formulae. The movements of the particles are guided by their own best known position in the search-space as well as the entire swarm's best known position. When improved positions are being discovered these will then come to guide the movements of the swarm.

In this project, the students are to use the PSO algorithm to derive state assignments that optimize the area, testability and power dissipation of the circuit. Functions for computing area, power and testability costs have been implemented. Students will generate results on benchmark circuits and will use an existing tool developed using the C language.

5. VHDL Modeling and Synthesis of Basic Data Path Building Blocks for FPGAs [2 Students]

In this project, students are required to develop VHDL models for basic data path building blocks including Register File with various requirements (single port, dual port), ALU, Shifter, Signed and Unsigned Multiplier. These models should be optimized to be synthesized on FPGAs utilizing FPGA resources. The students will study the existing resources of a Vertex 6 FPGA and will report their findings in terms of FPGA resources utilization. This project requires prior knowledge of VHDL.

Project Deadlines:

Task	Deadline
Project selection	Tuesday, Nov. 8
Project Plan	Tuesday, Nov. 30
Progress Report	Tuesday, Dec. 21
Final Report & Project Demonstration	Tuesday, Jan. 26

Each student group is expected to submit a project plan describing the project tasks, the time planned for each task, and the team members' role in each task. Each group is also required to submit a progress report describing briefly the progress made so far in the project against planned work, difficulties faced, results obtained so far and the tasks to be performed in the next period. At the end of the project, each group is required to submit a professional report showing the details of all the work performed and demonstrate their project to me.

Project Evaluation Criteria:

Task	Mark
Project Plan	5%
Progress Report	10%
Project Accomplishments vs. Requirements	60%
Final Report Documentation & Organization	25%