**Jan. 15, 2008**

# COMPUTER ENGINEERING DEPARTMENT

## COE 561

## Digital System Design and Synthesis

## MAJOR EXAM II

**(Open Book Exam)**

**First Semester (081)**

**Time: 12:00-2:30 PM**

Student Name : _____

Student ID. : _____

| Question | Max Points | Score |
|---|---|---|
| Q1 | 30 | |
| Q2 | 15 | |
| Q3 | 15 | |
| Q4 | 20 | |
| Q5 | 20 | |
| Total | 100 | |

**[30 Points]**

**(Q1)** Consider the function F(A, B, C, D) with **ON-SET=Σm(3, 4, 5, 7)** and **OFF-SET=Σm(1, 9, 10, 14)**. Note that you do not need to use the positional-cube notation in your solution.

**(i)** **Expand** the minterm **A'BC'D'** using ESPRESSO heuristics.

**(ii)** A cover of the function is given by F = A'B + A'C. **Reduce** the cube **A'C** using Theorem 7.4.1.

**(iii)** Use Corollary 7.4.1 to check if the implicant **A'C** is an **essential** prime implicant.

**[15 Points]**

**(Q2)** Consider the logic network defined by the following expression:

$$x = a\ b\ d\ e\ f + a\ c\ d\ e\ f + a\ b\ d\ e\ g + a\ c\ d\ e\ g$$

Using the recursive procedure **KERNELS**, compute all the kernels and co-kernels of *x*. Show all the steps of the algorithm. Assume the following lexicographic order: {a, b, c, d, e, f, g}.

**[15 Points]**

**(Q3)** Consider the logic network defined by the following expression:

$$x = a\ b\ d'\ e' + a'\ c'\ d'\ e' + a\ b'\ d + a\ b'\ e + a'\ c\ d + a'\ c\ e$$

Compute the weight of the double cube divisors $d_1 = a\ b + a'\ c'$ and $d_2 = d + e$. Extract the double cube divisor with the highest weight and show the resulting network after extraction and the number of literals saved.

**[20 Points]**

**(Q4)** Consider the logic network defined by the following expressions with inputs *{a, b, c}* and output {*y}*:

$$w = b'\, c\, a' + b\, c'$$

$$x = w \oplus c$$

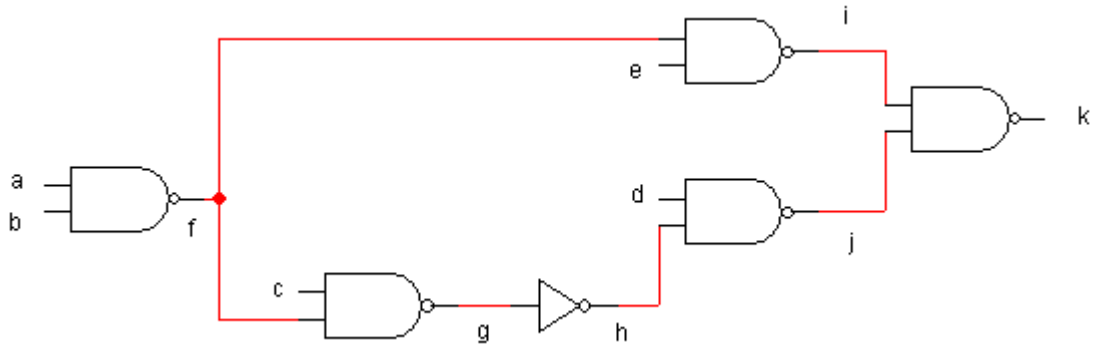
$$y = w\, b + w\, a + x$$

**(i)** Simplify the function *x* based on the utilization of don't care conditions.

**(ii)** Based on perturbation analysis, determine if it is possible to change the implementation of w to $w=b + c$.

**[20 Points]**

**(Q5)** Consider the logic network below with inputs *{a, b, c, d, e}* and output *{k}*:




Assume that the delay of the inverter gate is 1 and that the delay of the 2-input NAND gate is 2. Also, assume that the input data-ready times are zero except for input *a*, which is equal to 2.

**(i)** Compute the data ready times and slacks for all vertices in the network.

**(ii)** Determine the topological critical path.

**(iii)** Suggest an implementation of the function *k* using only inverters and 2-input NAND gates to reduce the delay of the circuit to the minimum possible and determine the maximum propagation delay in the optimized circuit. Has the area been affected?