Jan. 6, 2006

COMPUTER ENGINEERING DEPARTMENT

COE 561

Digital System Design and Synthesis

MAJOR EXAM II

(Open Book Exam)

First Semester (061)

Time: 7:30-9:30 PM

Student Name : _____

Student ID. : _____

Question	Max Points	Score
Q1	30	
Q2	25	
Q3	20	
Q4	25	
Total	100	

[30 Points]

(Q1) Consider the function F(A, B, C, D) with **ON-SET=Σm(0, 2, 3, 7, 10)** and **DC-SET=Σm(1, 6, 8, 14)**. Note that you do not need to use the positional-cube notation in your solution.

(i) **Expand** the minterm **AB'CD'** using ESPRESSO heuristics.

(ii) A cover of the function is given by F = A'C + B' D'. **Reduce** the cube **A'C** using Theorem 7.4.1.

(iii) Use Corollary 7.4.1 to check if the implicant **A'C** is an **essential** prime implicant.

[25 Points]

(Q2) Consider the logic network defined by the following expressions:

$$x = a\ b\ d + b'\ c\ d + c\ e + d\ e$$

$$y = a'\ b\ d' + b'\ c'\ d' + a'\ c'\ d' + c'\ d'\ e$$

(i) Using the procedure **KERNELS**, compute all the kernels and co-kernels of *x*. Show all the steps of the algorithm. Assume the following lexicographic order: {a, b, b', c, d, e}.

(ii) Compute the double-cube divisors of *x* and *y* and compute the **weight** of each double-cube divisor taking into account the combination of all divisors of *x* and *y*. **Extract** the best double-cube divisor and show the resulting network.

[20 Points]

(Q3) Consider the logic network defined by the following expressions:

$c = a'$

$x = a \cdot b$

$y = a \oplus b$

$w = x + y' + c'$

Inputs are $\{a, b\}$ and output is w.

(i) Compute the **CDC set** for the cut $\{x, y, c\}$. Simplify the equation of w to the minimum number of literals possible.

(ii) Compute **ODC set** for node x. Based on the ODC set of node x, decide if the fault **x stuck-at-0** is testable or not. If it is testable, find all tests detecting the fault. If it is untestable, optimize the network by eliminating redundancy.

[25 Points]

(Q4) Consider the logic network defined by the following expressions:

$k = a \cdot b$

$l = a \cdot c$

$h = a + c$

$e = a' + b$

$g = k + l$

$f = d' \cdot g$

$i = f \oplus d$

$x = e \oplus i$

$j = f + d$

$y = j + h$

Inputs are *{a, b, c, d}* and outputs are *{x, y}*. Assume that the delay of each inverter, AND and OR gates is 1 and that the delay of each XOR gate is 2. Also, assume that the input data-ready times are zero except for input *a*, which is equal to 2.

(i) Draw the logic network graph and compute the data ready times and slacks for all vertices in the network.

(ii) Determine the **maximum propagation delay** and the **topological critical path**.

(iii) Suggest an implementation of the function ***g*** in terms of the Inputs *{a, b, c}* to reduce the delay of the circuit. What is the **maximum propagation delay** after the modified implementation?