KING FAHD UNIVERSITY OF PETROLEUM & MINERALS  
*COMPUTER ENGINEERING DEPARTMENT*

**COE 561: Digital System Design and Synthesis**

**Term 111 Lecture Breakdown**

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| **Lec#** | **Date** | **Topics** | **Ref.** |
| 1 | S 10/9 | Syllabus, **Introduction**: Microelectronics Design Problems, Microelectronics Design Styles. | Chapter 1 |
| 2 | M 12/9 | Dealing with design complexity, Design domains and levels of abstractions, Digital system design, Design vs. synthesis. Digital system design cycle, Synthesis process, High-level synthesis. | Chapter 1 |
| 3 | S 17/9 | Design and evaluation space, Combinational design space example, Architecture design space example, Pareto Optimality. **Logic Synthesis Background**: Boolean Algebra, Boolean Functions, Shannon’s Theorem. | Chapter 1 & 2.5 |
| 4 | M 19/9 | Unate functions. Boolean difference, Consensus, Smoothing, Orthonormal Basis Expansion. Representation of Boolean functions, **Binary Decision Diagrams.** | 2.5 |
|  | S 24/9 | **National Day - Holiday** |  |
| 5 | M 26/9 | Reduced Binary Decision Diagrams, **ITE DAGs**. Applications of ITE DAGs. **Satisfiability**, Satisfiability Formulation as Zero-One Linear Programming (ZOLP) Problem, Minimum Covering Problem. | 2.5 |
| 6 | S 1/10 | Minimum-Vertex Cover Example, Minimum-Edge Cover Example,Covering Problem Formulated as Satisfiability Problem. **Branch & Bound Algorithm**. Covering reduction strategies. Branch and Bound Exact Covering Algorithm, Bounding function. | 2.5 |
| 7 | M 3/10 | **Two-level minimization**: Programmable Logic Arrays. Minimal or irredundant cover, Minimal cover w.r.t. 1-implicant containment. Prime implicant, Prime cover, Essential prime implicant. **Positional cube notation**, Operations on logic covers: intersection, supercube, distance, cofactor, Sharp. | Chapter 7 |
| 8 | S 8/10 | Disjoint Sharp, Consensus, Computation of all prime implicants. Tautology, Containment. Complementation. | Chapter 7 |
| 9 | M 10/10 | E**xact two-level minimization**, ESPRSSSO-EXACT. **Heuristic minimization**, Heuristic minimization operators: Expand, Reduce, Irredundant, Reshape. Expand heuristics. | Chapter 7 |
| 10 | S 15/10 | Expand heuristics, Reduce. | Chapter 7 |
| 11 | M 17/10 | Irredundant, Essentials. Espresso Algorithm. Testability of Two Level circuits. | Chapter 7 |
|  | W 19/10 | **Last Day for Dropping with W** |  |
|  | Th. 20/10 | **Major Exam I** |  |
| 12 | S 22/10 | Logic Network, Network optimization, Area Estimation. **Mutlilevel transformations**: Elimination, Decomposition, Factoring. | Chapter 8 |
| 13 | M 24/10 | Extraction, Simplification, Substitution. Elimination algorithm. **Algebraic model**. Algebraic division algorithm. Substitution algorithm, Extraction, Kernels, Kernels computation. | Chapter 8 |
| 14 | S 29/10 | **Kernel Set Computation**, Recursive Kernel Computation, Matrix Representation of Kernels. Single-Cube Extraction, Multiple-cube extraction.  Value of a Kernel. | Chapter 8 |
| 15 | M 31/10 | No Class. |  |
|  | 1-11/11 | **Id Al-Adha Vacation** |  |
| 16 | S 12/11 | **Decomposition**. **Factorization** Algorithm: quick & Good Factoring. **Fast Extraction** Algorithm: Double-cube divisors and single-cube divisors. Boolean Methods, Controllability & Observability don’t care conditions. **Satisfiability don’t care** conditions, Controllability don’t care computation. | Chapter 8 |
| 17 | M 14/11 | Observability don’t care conditions computation. Multi-Way Stems Theorem. Observability Don't Care Algorithm, Transformations with don’t cares. Optimization and perturbations. Synthesis and testability. | Chapter 8 |
| 18 | S 19/11 | Synthesis and testability, **Synthesis for testability**. Timing issues in multilevel logic optimization, **delay modeling**, topological critical path. | Chapter 8 |
| 19 | M 21/11 | False path problem. Algorithms for delay minimization, Transformations for delay reduction. More refined delay models, Speedup algorithm. | Chapter 8 |
|  | W 23/11 | **Last Day for Dropping all Courses with W** |  |
|  | Th. 24/11 | **1st Paper Presentation** |  |
| 20-21 | Th. 1/12 | **Library Binding**: Library Models, Major Approaches, Rule-based library binding. Algorithms for library binding, Partitioning, Decomposition, Matching, Covering. Tree-based matching. **Tree-based covering. Minimum Area Cover, Minimum Delay Cover**: constant delay, load-dependent delay. | Chapter 10 |
| 22-23 | Th. 8/12 | **Boolean matching**: Signatures and Filters. **Sequential Logic Synthesis**: Modeling Synchronous circuits, **State minimization** for completely and incompletely-specified FSMs. | Chapter 10 & 9 |
|  | M 12/12 | **Major Exam II** |  |
| 24 | S 17/12 | **State minimization** for incompletely-specified FSMs. **State** **Assignment**. State encoding for two-level models. Symbolic minimization, **Input encoding problem.** | Chapter 7 & 9 |
| 25 | M 19/12 | Dichotomy theory, Exact & Heuristic input encoding. **Output and mixed encoding**, Covering relation. | Chapter 7 & 9 |
| 26-27 | Th. 22/12 | **Output and mixed encoding**, Covering and Disjunctive relation. State encoding for two-level implementation. Limitation of Symbolic Minimization and Constrained Encoding, Synchronous logic network, **Retiming**. | Chapter 7 & 9 |
|  | S 24/12 | **Dropping all Courses with WP/WF** |  |
| 28-29 | Th. 29/12 | **Architectural-level synthesis**, Data-flow graphs, **Sequencing graphs**, Behavioral optimization of sequencing graphs. Synthesis in the temporal domain: **Scheduling**, Synthesis in the Spatial domain: **Binding.** Scheduling Models, Minimum latency unconstrained scheduling, ASAP & ALAP scheduling, Latency Constrained Scheduling, Scheduling under Resource Constraints. ILP Formulation,List Scheduling Algorithm for Minimum Latency, List Scheduling Algorithm for Minimum Resource Usage. | Chapter 3 & 4 & 5 |
|  | Th. 5/1 | **2nd Paper Presentation** |  |
| 30 | Th. 5/1 | Algorithmic Solution to the Optimum Binding Problem, ILP Formulation of Binding, Register Binding Problem. Left-Edge Algorithm. | Chapter 6 |