Name: **Id#**

COE 405, Term 181

Design & Modeling of Digital Systems

Quiz# 6 Solution

Date: Sunday, Dec. 9, 2018

Q.1. Fill in the blank in each of the following questions:

(1) Three advantages of using FPGAs over ASICs are low development cost, short time to market ad reconfigurability.

(2) Two types of FPGA technologies are SRAM-based FPGAs and Flash and Anti-Fuse FPGAs.

(3) In FPGAs, each configurable logic block (CLB) has a number of the following two main blocks: look-up tables (LUT) and Flip Flops.

(4) Each IOB can be configured to work as uni-directional I/O or bi-directional I/O.

(5) Modern FPGAs, in addition to having CLBs and IOBs, have the following components: Block RAMs, Multipliers, Clock Management, Gigabit serial.

(6) In FPGAs, memory can be implemented in two ways either as distributed RAM using LUTs or using Block RAM.

(7) The difference between simple dual port and true dual port RAM is that is simple dual port ram has one read-only port and one read/write port while in true dual port both ports could be either read or write.

(8) To have a RAM with synchronous read, the RAM must be implemented using either distributed RAM (i.e. using LUTs) or using BRAM.

(9) Using a Block RAM with Read_First write mode means that when the memory is written it will output the previously stored data while new data is being written.

(10) Using a Block RAM with No_Change write mode means that when the memory is written it will maintain the output previously generated by a read operation.

Q.2. Write a parametrizable Verilog model for modeling a memory with a simple dual port memory with synchronous read and write by completing the following module:

```
module Memory_Unit#(parameter word_size=8, address_size=8, memory_size=256)(
output  reg [word_size-1:0] data_out1,
output reg [word_size-1:0] data_out2,
input [word_size-1:0] data_in,
input [address_size-1:0] address1,
input [address_size-1:0] address2,
input clk, write);

reg [word_size-1:0] memory[memory_size-1:0];

always @ (posedge clk) begin
  if (write) memory[address1] <= data_in;
  else data_out1 <= memory[address1];
  data_out2 <= memory[address2];
end
endmodule
```

Q.3. Consider the logic network defined by the following expression:

$$x = a\,b\,d'\,e' + a'\,c'\,d'\,e' + a\,b'\,d + a\,b'\,e + a'\,c\,d + a'\,c\,e$$

Compute the weight of the double cube divisors $d_1 = a\,b + a'\,c'$ and $d_2 = d + e$. Extract the double cube divisor with the highest weight and show the resulting network after extraction and the number of literals saved.

Double Cube Divisor	Base
$d_1 = ab + \bar{a}\bar{c}$	$\bar{d}\bar{e}$
$\bar{d}_1 = a\bar{b} + \bar{a}c$	d, e
$d_2 = d + e$	$a\bar{b}, \bar{a}c$

weight(d_1) = $3 * 4 - 3 - 4 + 2 + 1 + 1 = 9$

weight(d_2) = $2 * 2 - 2 - 2 + 2 + 2 + 2 = 6$

Since d_1 has a higher weight, it will be extracted.

The resulting network after extracting d_1 is:

$d_1 = ab + \bar{a}\bar{c}$

$x = d_1\bar{d}\bar{e} + \bar{d}_1 d + \bar{d}_1 e$ 11 literals

Number of literals saved = 9.