Name: **Id#**

COE 405, Term 181

Design & Modeling of Digital Systems

Quiz# 6

Date: Sunday, Dec. 9, 2018

Q.1. Fill in the blank in each of the following questions:

(1) Three advantages of using FPGAs over ASICs are _____ _____.

(2) Two types of FPGA technologies are _____ _____.

(3) In FPGAs, each configurable logic block (CLB) has a number of the following two main blocks: _____.

(4) Each IOB can be configured to work as _____ or _____.

(5) Modern FPGAs, in addition to having CLBs and IOBs, have the following components: _____.

(6) In FPGAs, memory can be implemented in two ways either as _____ _____ or using _____.

(7) The difference between simple dual port and true dual port RAM is that _____ _____ _____.

(8) To have a RAM with synchronous read, the RAM must be implemented using _____.

(9) Using a Block RAM with Read_First write mode means that when the memory is written it will _____.

(10) Using a Block RAM with No_Change write mode means that when the memory is written it will _____.

Q.2. Write a parametrizable Verilog model for modeling a memory with a simple dual port memory with synchronous read and write by completing the following module:

```
module Memory_Unit#(parameter word_size=8, address_size=8, memory_size=256)(
output  reg [word_size-1:0] data_out1,
output reg [word_size-1:0] data_out2,
input [word_size-1:0] data_in,
input [address_size-1:0] address1,
input [address_size-1:0] address2,
input clk, write);
```

Q.3. Consider the logic network defined by the following expression:

$$x = a\ b\ d'\ e' + a'\ c'\ d'\ e' + a\ b'\ d + a\ b'\ e + a'\ c\ d + a'\ c\ e$$

Compute the weight of the double cube divisors $d_1 = a\ b + a'\ c'$ and $d_2 = d + e$. Extract the double cube divisor with the highest weight and show the resulting network after extraction and the number of literals saved.