

Name:

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COE 405, Term 162

Design & Modeling of Digital Systems

Quiz# 5 Solution

Date: Tuesday, May 16, 2017

Q1. Consider the logic network defined by the following expressions:

$$g = a b$$

$$h = a' b'$$

$$i = g + h$$

$$j = c d$$

$$k = i j e$$

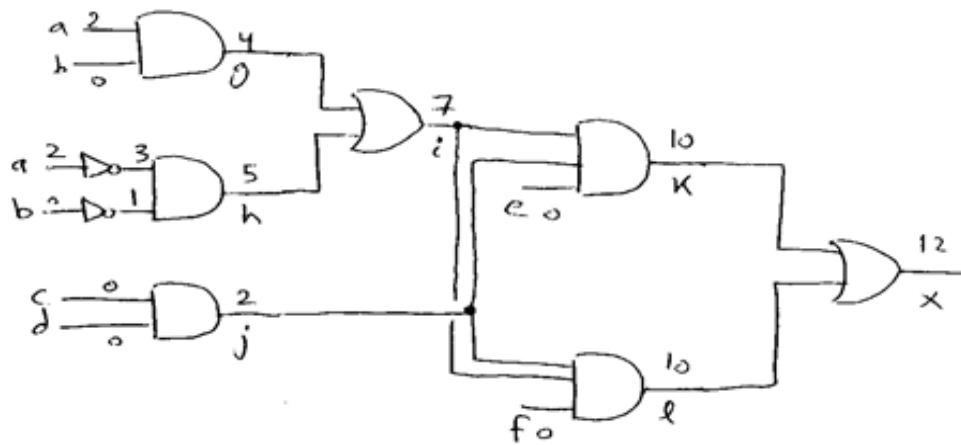
$$l = i j f$$

$$x = k + l$$

Inputs are $\{a, b, c, d, e, f\}$ and output is $\{x\}$. Assume that the delay of a gate is related to the number of its inputs. Also, assume that the input data-ready times are zero except for input a , which is equal to 2.

- (i) Draw the logic network graph and compute the data ready times and slacks for all vertices in the network.
- (ii) Determine the **maximum propagation delay** and the **topological critical path**.
- (iii) Suggest an implementation of the function x to reduce the delay of the circuit. What is the **maximum propagation delay** after the modified implementation? Has the area been impacted?

(i)



The data ready times are shown on the figure.

The maximum propagation delay is 12.

To compute the slack for each node, the required time for x is set to 12.

$$\bar{t}_x = 12, \quad S_x = 12 - 12 = 0$$

$$\bar{t}_k = 12 - 2 = 10, \quad S_k = 10 - 10 = 0$$

$$\bar{t}_l = 12 - 2 = 10, \quad S_l = 10 - 10 = 0$$

$$\bar{t}_i = \min\{10 - 3, 10 - 3\} = 7, \quad S_i = 7 - 7 = 0$$

$$\bar{t}_j = \min\{10 - 3, 10 - 3\} = 7, \quad S_j = 7 - 2 = 5$$

$$\bar{t}_g = 7 - 2 = 5, \quad S_g = 5 - 4 = 1$$

$$\bar{t}_h = 7 - 2 = 5, \quad S_h = 5 - 5 = 0$$

$$\bar{t}_a = \min\{5 - 2, 5 - 2 - 1\} = 2, \quad S_a = 2 - 2 = 0$$

$$\bar{t}_b = \min\{5 - 2, 5 - 2 - 1\} = 2, \quad S_b = 2 - 0 = 2$$

$$\bar{t}_c = 7 - 2 = 5, \quad S_c = 5 - 0 = 5$$

$$\bar{t}_d = 7 - 2 = 5, \quad S_d = 5 - 0 = 5$$

$$\bar{t}_e = 10 - 3 = 7, \quad S_e = 7 - 0 = 7$$

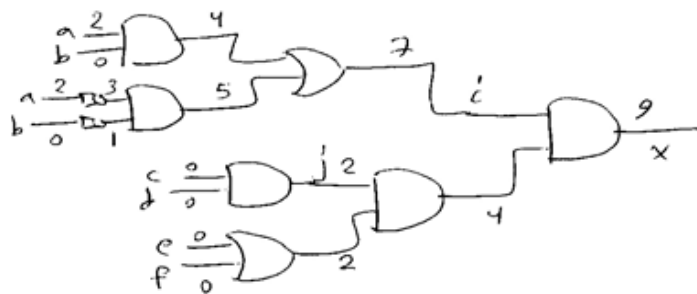
$$\bar{t}_f = 10 - 3 = 7, \quad S_f = 7 - 0 = 7$$

(ii) Maximum propagation delay = 12

Topological critical Paths :

$\{a, h, i, x, x\}$, $\{a, h, i, l, x\}$

(iii) Since i is the one affecting the critical path, we need to bring it closer to the output. Thus, the improved implementation is as follows:



Thus, delay of x is reduced from 12 to 9. At the same time, the area of the circuit has improved.