Name: **Id#**

COE 405, Term 162

Design & Modeling of Digital Systems

Quiz# 5

Date: Tuesday, May 16, 2017

Q1. Consider the logic network defined by the following expressions:

g = a b

h = a' b'

i = g + h

j = c d

k = i j e

l = i j f

x =k + l

Inputs are {a, b, c, d, e, f} and output is {x}. Assume that the delay of a gate is related to the number of its inputs. Also, assume that the input data-ready times are zero except for input a, which is equal to 2.

(i) Draw the logic network graph and compute the data ready times and slacks for all vertices in the network.

(ii) Determine the **maximum propagation delay** and the **topological critical path**.

(iii) Suggest an implementation of the function ***x*** to reduce the delay of the circuit. What is the **maximum propagation delay** after the modified implementation? Has the area been impacted?