Name: **Id#**

<center>

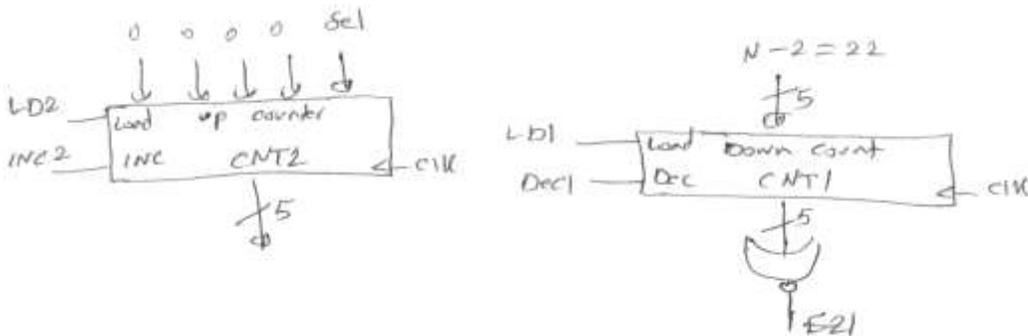**COE 405, Term 181**

Design & Modeling of Digital Systems

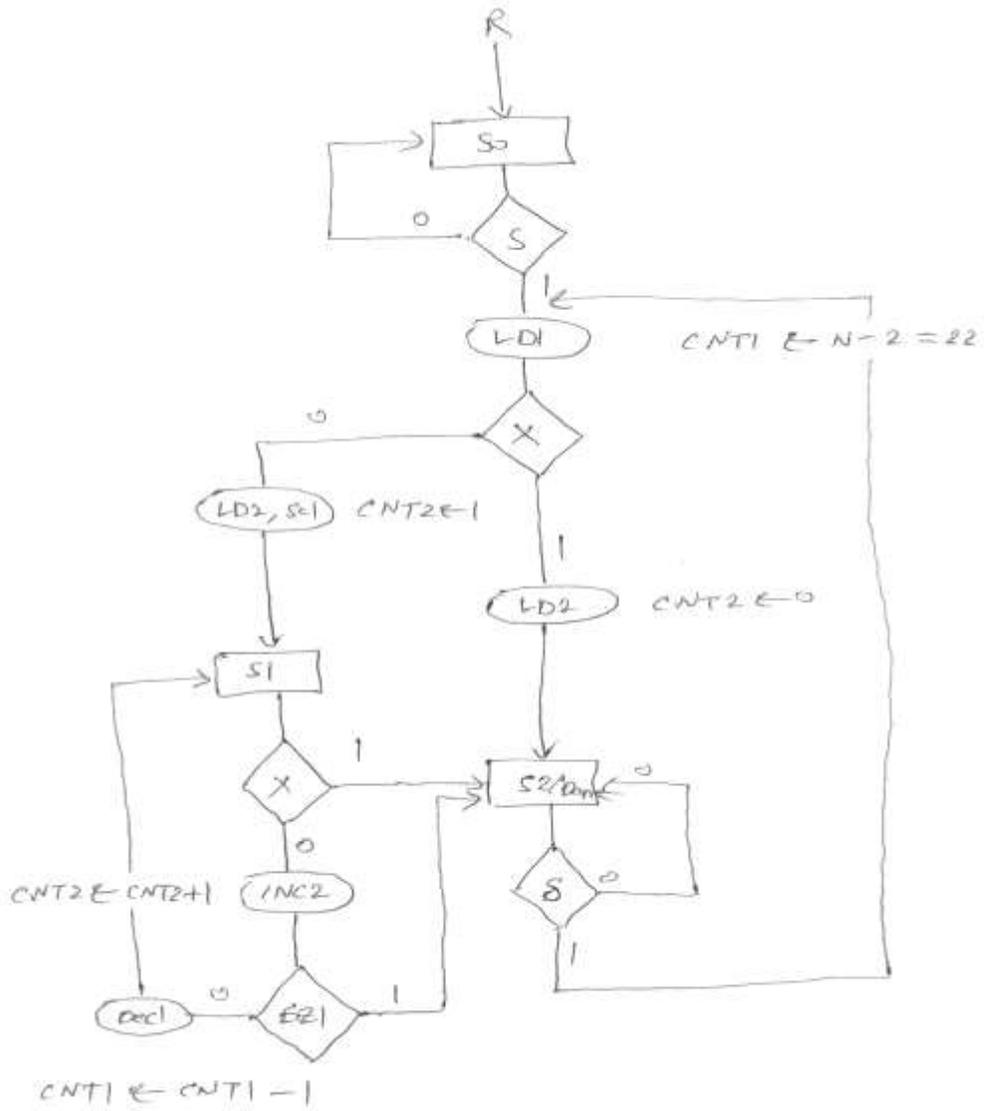**Quiz# 4 Solution**

Date: Tuesday, Nov. 13, 2018

</center>

Q.1.   It is required to design a circuit that counts the number of leading zeros in a 24-bit data that is sent serially from the most significant bit to the least significant bit. The data is applied serially through an input X once the user presses a Start button, where the first bit is transmitted in the same cycle the Start button is asserted. The circuit should assert a Done signal **as soon as** the computation is completed, which remains asserted until the user presses the Start button again or resets the machine. Assume that the machine has Asynchronous Reset input. For example, if the data 00101…1 is sent the circuit should indicate that the number of leading zeros is 2.

   (i)   Show the block diagram design of the data path, showing components sizes and their control signals.

(ii) Show the ASM chart for this circuit.

R

S0

0 → S

LD1 $CNT1 \leftarrow N-2 = 22$

X

LD2, Sel $CNT2 \leftarrow 1$

LD2 $CNT2 \leftarrow 0$

S1

X

$CNT2 \leftarrow CNT2+1$ INC2

S2/Done

8

Dec1   EZ1

$CNT1 \leftarrow CNT1 - 1$

Timing Diagram :   N=3   (assuming 3 bits)

clk				
S0		S1	S1	S2
x=0		x=0	x=0	
S				
CNT1			0	0
CNT2			2	3
				Done