

Name: KEY

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COE 405, Term 031

Design & Modeling of Digital Systems

Quiz# 4

Date: Tuesday, Dec. 23, 2003

Q.1. Given the following Entity Description for a JK Flip-Flop:

```
ENTITY JKFF IS
  GENERIC (delay : TIME := 4 NS);
  PORT (j, k, clk, reset : IN BIT; q, qb : OUT BIT);
END JKFF;
```

- (i) Model the JK-FF using a BLOCK statement with a GUARD expression and conditional signal assignment, assuming that reset is synchronous and the JK-FF is rising-edge triggered.

```
Architecture Sreset of JKFF is
begin
  edge: BLOCK ( clk = '1' AND NOT clk'STABLE )
  BEGIN
    q <= GUARDED '0' after delay when reset = '1' else '1' after delay when
    j='1' and k='0' else '0' after delay when j='0' and k='1' else not q after delay
    when j='1' and k='1' else q;
    qb <= NOT q;
  END BLOCK;
end Sreset;
```

- (ii) Model the JK-FF using a BLOCK statement with a GUARD expression and selective signal assignment, assuming that reset is synchronous and the JK-FF is rising-edge triggered.

```
Architecture Sreset2 of JKFF is
  signal s : bit_vector(2 downto 0);
begin

  s <= reset & j & k;
```

```

edge: BLOCK ( clk = '1' AND NOT clk'STABLE )
  BEGIN
    with s select
      q <= GUARDED '0' after delay when "001",
        '1' after delay when "010",
        not q after delay when "011",
        q after delay when "000",
        '0' after delay when others;
      qb <= NOT q;
    END BLOCK;
  end Sreset2;

```

- (iii) Model the JK-FF using a BLOCK statement with a GUARD expression and conditional signal assignment, assuming that reset is asynchronous and the JK-FF is rising-edge triggered.

Architecture ASreset of JKFF is
begin

```

edge: BLOCK ( reset='1' OR (clk = '1' AND NOT clk'STABLE ) )
  BEGIN
    q <= GUARDED '0' after delay when reset = '1' else '1' after delay when
j='1' and k='0' else '0' after delay when j='0' and k='1' else not q after delay when
j='1' and k='1' else q;
    qb <= NOT q;
  END BLOCK;

end ASreset;

```