

Name:

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COE 405, Term 162

Design & Modeling of Digital Systems

Quiz# 4

Date: Tuesday, May 1, 2017

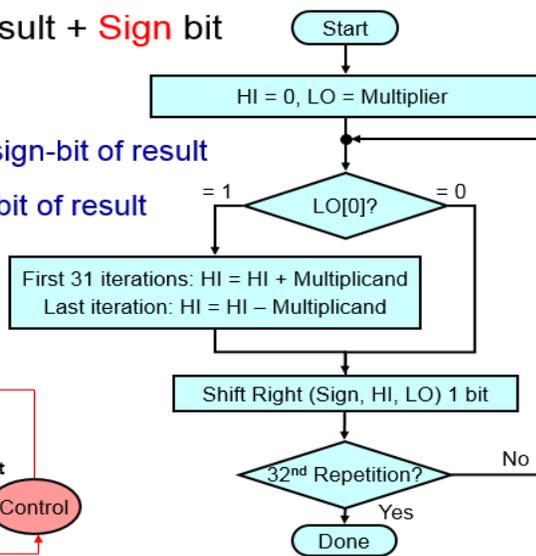
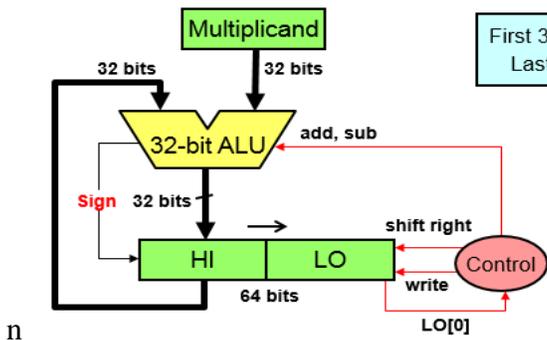
Q1. It is required to design an **n-bit signed multiplier** circuit. The architecture and the algorithm for performing signed multiplication are given below:

❖ ALU produces **32-bit result + Sign bit**

❖ **Sign bit** set as follows:

❖ **No overflow** → **Extend sign-bit** of result

❖ **Overflow** → **Invert sign-bit** of result



Write a parametrizable Verilog module to model the signed multiplication circuit as a combinational circuit using for loop.

