Name: **Id#**

COE 405, Term 152

Design & Modeling of Digital Systems

Quiz# 4

Date: Sunday, April 14, 2016

Q.1. It is required to design a circuit that receives two **4-bit** signed numbers in 2's complement representation $\mathbf{A=A_3A_2A_1A_0}$, $\mathbf{B=B_3B_2B_1B_0}$ and produces a **<u>6-bit output</u>** $\mathbf{C=C_5C_4C_3C_2C_1C_0}$. The circuit implements the following functions based on the values of the three selection inputs: S1, S1 and S0.

S2 S1 S0	Function
0 0 0	C = A + B
0 0 1	C = A - B
0 1 0	C = A + 1
0 1 1	C = A - 1
1 0 0	C = 2*A+B
1 0 1	C = 2*A-B
1 1 0	C = 2*A+1
1 1 1	C = 2*A-1

(i) Show the block diagram design of your circuit using MSI components like Adder, Multiplexor, as needed. Use only one adder in your solution.

(ii) Model your design in Verilog by modeling each component separately i.e. adder, MUX, etc. and then instantiate these components to model your circuit.

(iii) Write a Behavioral Verilog model to model the given circuit.