Name: **Id#**

COE 405, Term 031

Design & Modeling of Digital Systems

Quiz# 4

Date: Tuesday, Dec. 23, 2003

Q.1. Given the following Entity Description for a JK Flip-Flop:

```
ENTITY JKFF IS
GENERIC (delay : TIME := 4 NS);
PORT (j, k, clk, reset : IN BIT; q, qb : OUT BIT);
END JKFF;
```

(i) Model the JK-FF using a BLOCK statement with a GUARD expression and conditional signal assignment, assuming that reset is synchronous and the JK-FF is rising-edge triggered.

(ii) Model the JK-FF using a BLOCK statement with a GUARD expression and slective signal assignment, assuming that reset is synchronous and the JK-FF is rising-edge triggered.

(iii) Model the JK-FF using a BLOCK statement with a GUARD expression and conditional signal assignment, assuming that reset is asynchronous and the JK-FF is rising-edge triggered.