Name: **Id#**

COE 405, Term 031

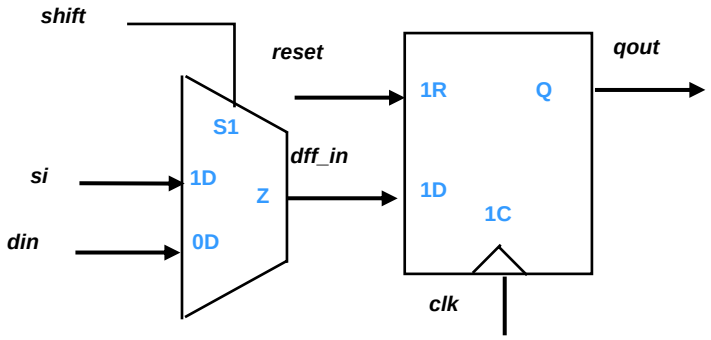
Design & Modeling of Digital Systems

Quiz# 3

Date: Sunday, Nov. 30, 2003

Q.1. It is required to model in VHDL a parametrizable **n-bit *Shift Right Register***. The register has a **shift** control input that when enabled it makes the register shift its content to the right. Assume that the value shifted to the most significant bit is taken from the input **SI**. Otherwise, the register will be loaded by an external input **DI**. Assume that register is rising-edge triggered and that it has an Asynchronous reset. Assume that you have the following SFF entity in the work library. Assume that SFF is rising-edge triggered and that its reset is Asynchronous. When shift=0, the SFF is loaded with din otherwise it is loaded with si.

```
Entity SFF IS
        PORT (din, si, shift, reset, clk: IN BIT; qout: OUT BIT);
END SFFf;
```



(i) Describe the entity of the n-bit shift register using GNERIC for passing the shift register size.

(ii) Model architecture for the n-bit shift register using GENERATE statement.