Name: **Id#**

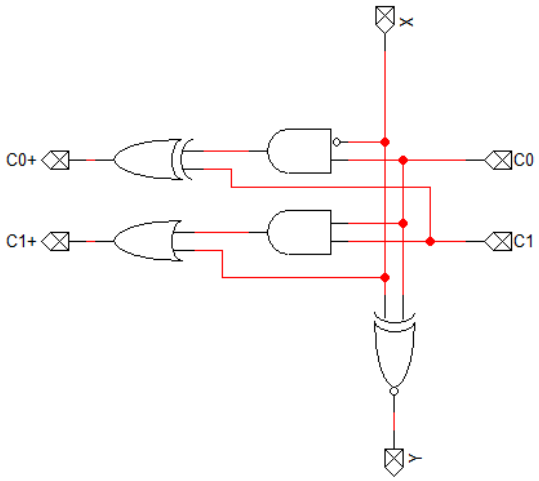
COE 405, Term 162

Design & Modeling of Digital Systems

Quiz# 2 Solution

Date: Tuesday, March 14, 2017

Q.1. Consider the combinational circuit given below modeling a 1-bit cell for computing the equation Y=3*X-1, which has three inputs C1, C0, and X and three outputs C1+, C0+ and Y:



(i) Write a Verilog model to model the 1-bit cell design of the circuit using either primitive gates or assign statement.

```
module Cell3XM1 (output C1P, C0P, Y, input C1, C0, X);

    assign Y = X ~^  C0;

    assign C0P = C1 ^ (~X &  C0);

    assign C1P = X | (C1 &  C0);

endmodule
```

(ii) Write a Verilog model for modeling a 3-bit circuit for computing the equation Y=3*X-1 by instantiating three copies of this cell and connecting C1 and C0 of the

first cell to 00, C1+ and C0+ of the first cell to C1 and C0 of the 2nd cell, C1+ and C0+ of the 2nd cell to C1 and C0 of the 3rd cell.

```
module D3XM1 (output C1, C0, output [2:0] Y, input [2:0] X);

wire  [1:0] C1P, C0P;

Cell3XM1 M1 (C1P[0], C0P[0], Y[0], 0, 0, X[0]);
Cell3XM1 M2 (C1P[1], C0P[1], Y[1], C1P[0], C0P[0], X[1]);
Cell3XM1 M3 (C1, C0, Y[2], C1P[1], C0P[1], X[2]);

endmodule
```

(iii) Write a test bench that tests your 3-bit circuit by applying the following input patterns to your cell (X2X1X0)={000, 001, 010, 111} and observing the obtained outputs Y2Y1Y0.

```
module D3XM1_Test();

reg [2:0] X;
wire C1, C0;
wire [2:0] Y;

D3XM1 M1 (C1, C0, Y, X);

initial begin
X=3'b000;
#100 X=3'b001;
#100 X=3'b010;
#100 X=3'b0111;
end

endmodule
```

Q.2. It is required to design a sequential circuit using Mealy model that computes the equation Y=X-3, where X is an unsigned number that will be fed serially. Assume that the circuit has an asynchronous Reset input that resets the machine to the reset state. Draw the state diagram or state table for your sequential circuit. Make sure that your state machine is minimal and that it does not have any redundant state.

Present State	**Next State, Y**	
	X=0	**X=1**
S0 (B=3)	S1, 1	S2, 0
S1 (B=2)	S2, 0	S2, 1
S2 (B=1)	S2, 1	S3, 0
S3 (B=0)	S3, 0	S3, 1

OR:

Present State	**Next State, Y**	
	X=0	**X=1**
S0 (C=0)	S1, 1	S2, 0
S1 (C=1)	S2, 0	S2, 1
S2 (C=2)	S2, 1	S3, 0
S3 (C=3)	S3, 0	S3, 1