Name: KEY **Id#**

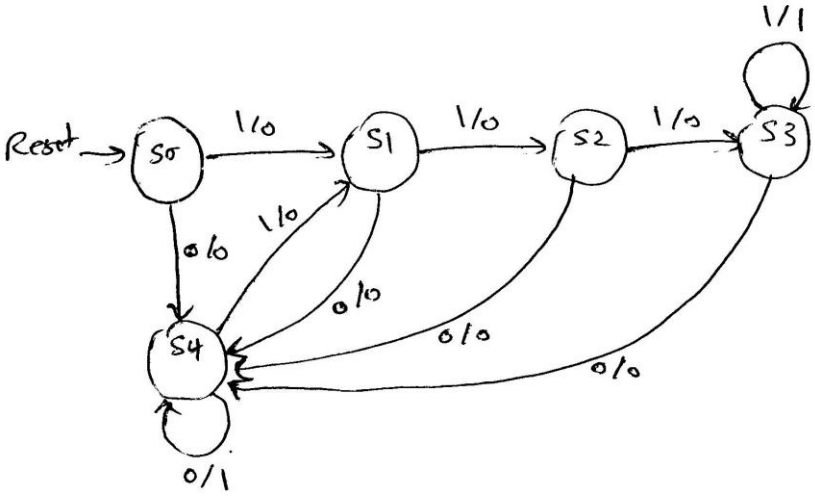
COE 405, Term 122

Design & Modeling of Digital Systems

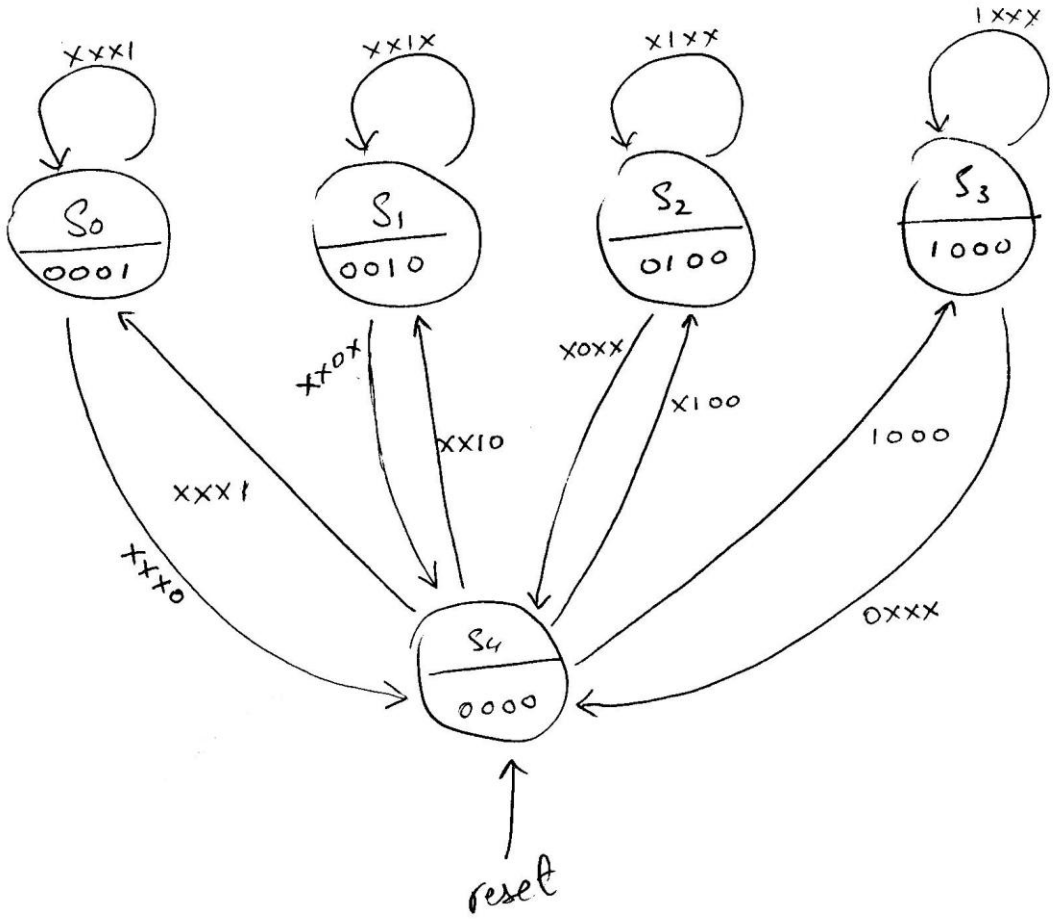
Quiz# 2

Date: Saturday, March 9, 2013

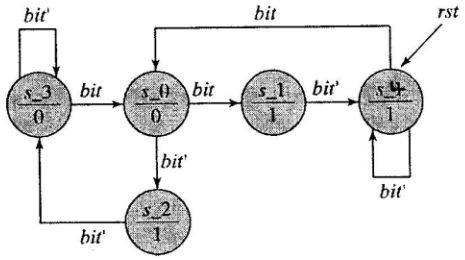
Q.1. Design a sequential circuit that has a single input X and a single output Z. The circuit produces a 1 output iff there have been four or more consecutive 1 inputs or two or more consecutive 0 inputs. Draw the state diagram of the circuit assuming a **Mealy** model. *You are not required to derive the equations and the circuit*.



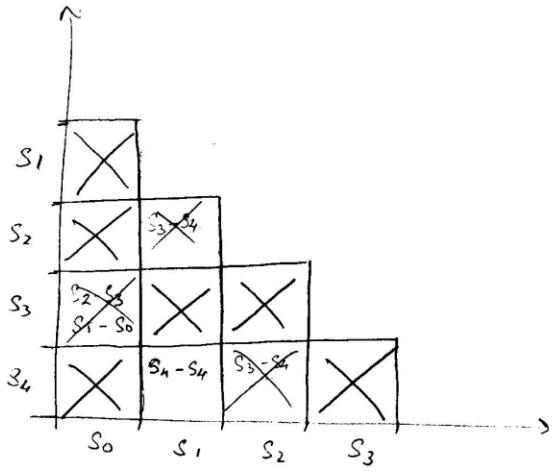
Q.2. Design a sequential bus controller that receives requests on separate lines, R0 to R3 from four devises desiring to use the bus. It has four outputs G0 to G3, only one of them is 1 indicating which device is granted control of the bus for that clock period. Assume that the low number device has the highest priority, if more than one device requests the bus at the same time. Assume that a device keeps control of the bus once it gets it until it no longer requests it. Also assume that the controller returns to the idle state for one clock period between bus allocations to different devices. Draw the <u>state diagram</u> of the circuit assuming a **<u>Moore</u>** model. *You are not required to derive the equations and the circuit*.



Q.3. Find the equivalent states of the STG shown below, and draw the STG of the reduced machine.



Current state	input	next state	output
S_0	0	S_2	0
S_0	1	S_1	0
S_1	0	S_4	1
S_1	1	X	1
S_2	0	S_3	1
S_2	1	X	1
S_3	0	S_3	0
S_3	1	S_0	0
S_4	0	S_4	1
S_4	1	S_0	1



∴ equivalent states.

$S_1 = S_4$.

S.T.G of reduced machine. ⟹