Name: KEY **Id#**

COE 405, Term 062

Design & Modeling of Digital Systems

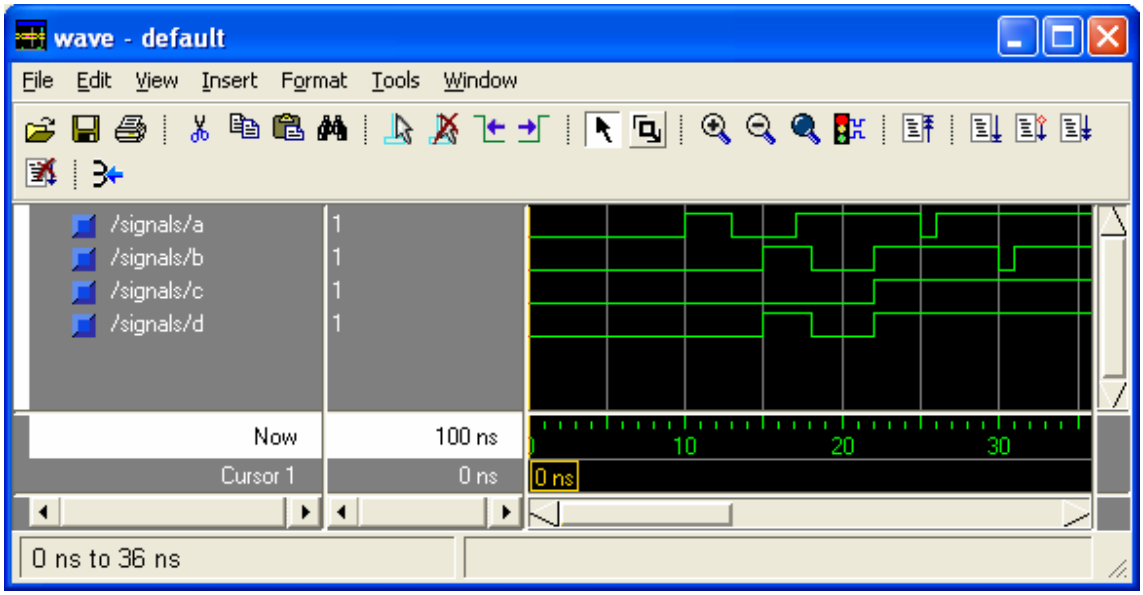
Quiz# 2

Date: Monday, March 26, 2007

Q.1. Given the following signal assignments, show all transactions placed on each signal. At each event, show transactions that are appended, overwritten, and expired including those occurring at delta time. Show resulting waveforms on each signal.

```
Architecture dataflow of signals IS
    Signal A, B, C, D: Bit := '0';
Begin
  A <= '1' after 10ns, '0' after 13ns, '1' after 17 ns, '0' after 25 ns, '1' after 26 ns;
  B <= transport A after 5ns;
  C <= A after 5 ns;
  D <= Reject 2 ns Inertial A after 5 ns;
End dataflow;
```

		0ns	5ns	10ns	13ns	15ns	17ns	18ns	22ns	25ns	26ns	30ns	31ns
A	Current Value	0	0	1	0	0	1	1	1	0	1	1	1
	Projected Waveform	(1,10) (0,13) (1,17) (0,25) (1,26)	(1,5) (0,8) (1,12) (0,20) (1,21)	(0,3) (1,7) (0,15) (1,16)	(1,4) (0,12) (1,13)	(1,2) (0,10) (1,11)	(0,8) (1,9)	(0,7) (1,8)	(0,3) (1,4)	(1,1)	ϕ	ϕ	ϕ
B	Current Value	0	0	0	0	1	1	0	1	1	1	0	1
	Projected Waveform	(0,5)	ϕ	(1,5)	(1,2) (0,5)	(0,3)	(0,1) (1,5)	(1,4)	ϕ	(0,5)	(0,4) (1,5)	(1,1)	ϕ
C	Current Value	0	0	0	0	0	0	0	1	1	1	1	1
	Projected Waveform	(0,5)	ϕ	(1,5)	~~(1,2)~~ (0,5)	(0,3)	~~(0,1)~~ (1,5)	(1,4)	ϕ	(0,5)	~~(0,4)~~ (1,5)	(1,1)	ϕ
D	Current Value	0	0	0	0	1	1	0	1	1	1	1	1
	Projected Waveform	(0,5)	ϕ	(1,5)	(1,2) (0,5)	(0,3)	(0,1) (1,5)	(1,4)	ϕ	(0,5)	~~(0,4)~~ (1,5)	(1,1)	ϕ



Q.2. You are required to model an N-bit 2x1 MUX. The MUX entity declaration is given below:

```
Entity MUXN2x1 is
        Generic(N : Natural :=8);
        PORT (A, B : IN Bit_Vector(N-1 Downto 0);
            S: IN Bit;
            C: OUT Bit_Vector(N-1 Downto 0)
            );
End;
```

(i) Model a single-bit 2x1 MUX using behavioral model.

```
Entity MUX2x1 is
        PORT (A, B, S: IN BIT; C: OUT BIT);
ENd;
Architecture Behavioral of MUX2x1 is
Begin
        Process(A, B, S)
        Begin
                if (S='0') Then
                        C <= A ;
                else
                        C <= B;
                end if;

        End Process;

End;
```

(ii) Using the model developed in (i) for the single-bit 2x1 MUX, develop a structural model for the N-bit 2x1 MUX using **generate** statement.

```
Entity MUXN2x1 is
        Generic(N : Natural :=8);
        PORT (A, B : IN Bit_Vector(N-1 Downto 0);
            S: IN Bit;
            C: OUT Bit_Vector(N-1 Downto 0)
            );
End;
Architecture Structural of MUXN2x1 is
Component MUX2x1
        PORT (A, B, S: IN BIT; C: OUT BIT);
ENd component;
Begin

MG: For I IN 0 To N-1 Generate
        MG: MUX2x1 port map (A(I), B(I), S, C(I));
   END Generate;

End;
```