Name: **Id#**

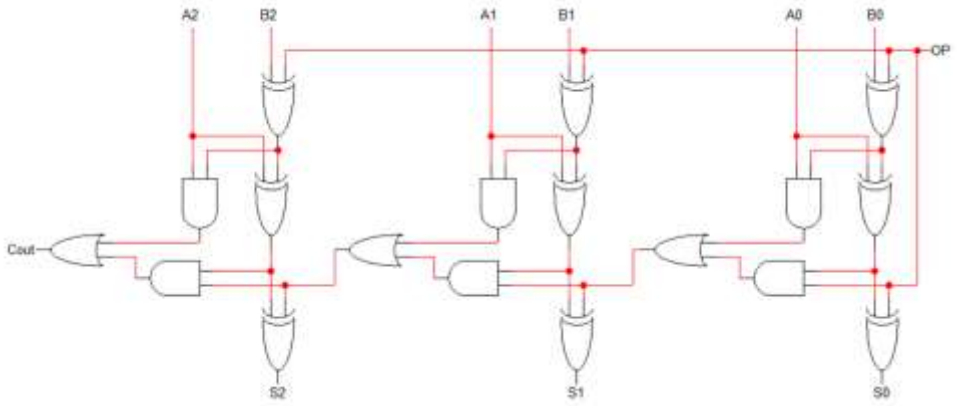
COE 405, Term 181

Design & Modeling of Digital Systems

Quiz# 2

Date: Sunday, October 7, 2018

Q.1. The circuit given below is a 3-bit adder/subtractor. The circuit performs addition when OP=0 and performs subtraction otherwise.



(i) Write a Verilog model to model a 1-bit cell design of the circuit using either primitive gates or assign statement.

(ii) Write a parametrizable Verilog model for modeling an n-bit adder/subtractor circuit using generate loop construct.

(iii) Write a test bench that instantiates and tests a 3-bit adder/subtractor circuit by applying the following input patterns to your circuit with a delay of 30 unit delays between successive input patterns: {(A=1, B=5, OP=0), {(A=1, B=5, OP=1), (A=7, B=7, OP=0), (A=0, B=7, OP=1)}.