Name: **Id#**

COE 405, Term 131

Design & Modeling of Digital Systems

Quiz# 2

Date: Thursday, October 24, 2013

Q.1. It is required to design a sequential circuit that has a single input X and a single output Y. The circuit receives an unsigned number serially through the input X from the least significant bit (LSB) to the most significant bit (MSB), and computes the equation Y=3*X+2 and generates the output serially from the least significant bit to the most significant bit. The circuit has an additional reset input R which resets the circuit into an initial state. The following are examples of input and output data:

Examples:

		LSB				MSB	
Input	X	0	1	1	0	0	Input=6
Output	Y	0	0	1	0	1	Output=20

		LSB				MSB	
Input	X	1	1	0	0	0	Input=3
Output	Y	1	1	0	1	0	Output=11

Draw the state diagram of the circuit assuming a **Mealy** model.

Q.2. Consider the following state table for an FSM which has a single input X, a single output Z:

Q_A	Q_B	X	Q_A^+	Q_B^+	Z
0	0	0	0	1	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	0	0	1
1	1	0	1	0	0
1	1	1	0	1	0

Implement the circuit for the FSM using D-FFs with minimal area.

Q.3. Consider the given FSM that has 5 states, one input (X) and one output (Z), represented by the following state table:

Present State	**Next State, Z**	
	X=0	**X=1**
S0	S3, 0	S0, 0
S1	S4, 0	S0, 0
S2	S3, 0	S1, 0
S3	S2, 1	S2, 0
S4	S2, 1	S1, 0

(i) Determine the equivalent states.

(ii) Reduce the state table into the minimum number of states and show the reduced state table.