**Name:** **Id#**

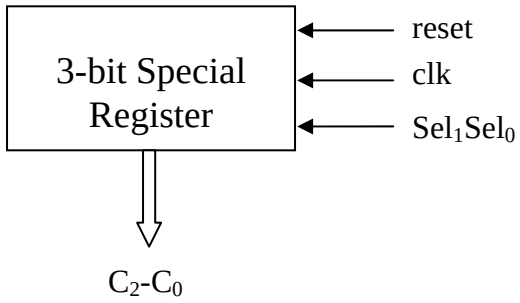
# COE 405, Term 031

## Design & Modeling of Digital Systems

## Quiz# 2

Date: Sunday, Nov. 2, 2003

**Q.1.** It is required to design a 3-bit register that has the capability to count up, count down, shift left logically, or shift right logically based on a 2-input select. The interface description of the 3-bit register is shown below, where **sel** determines the operation. When sel=00, the register will count up, when sel=01, it will count down, when sel=10, it will shift left logically, and when sel =11, it will shift right logically. The reset is an **asynchronous reset** and the register is **rising-edge** triggered.




**(i)** Describe an Entity **CS3** for the 3-bit register using type BIT and BIT_VECTOR for the interface signals.

**(ii)** Model a behavioral Architecture **Behave** for this 3-bit register.

**Q.2.** Given the following signal assignments, show all transactions placed on each signal. At each event, show transactions that are appended, overwritten, and expired including those occurring at delta time. Show resulting waveforms on each signal.

```
Architecture dataflow of signals IS
    Signal A, B, C, D: Bit := '0';
Begin
  A <= '1' after 10ns, '0' after 13ns, '1' after 17 ns, '0' after 25 ns, '1' after 26 ns;
  B <= transport A after 5ns;
  C <= A after 5 ns;
  D <= Reject 2 ns Inertial A after 5 ns;
End dataflow;
```