Name: **Id#**

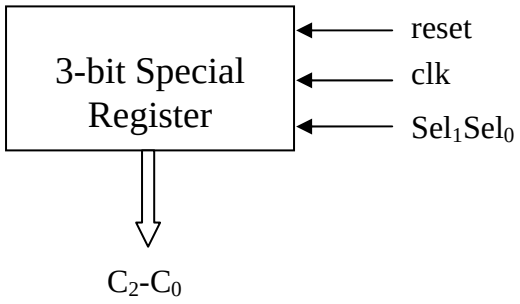
COE 405, Term 021

Design & Modeling of Digital Systems

Quiz# 2

Date: Monday, October 21, 2002

Q.1. It is required to design a 3-bit register that has the capability to count up, count down, shift left logically, or shift right logically based on a 2-input select. The interface description of the 3-bit register is shown below, where **sel** determines the operation. When sel=00, the register will count up, when sel=01, it will count down, when sel=10, it will shift left logically, and when sel =11, it will shift right logically. The reset is a synchronous reset and the register is rising-edge triggered.



(i) Describe an Entity **CS3** for the 3-bit register using type BIT and BIT_VECTOR for the interface signals.

(ii) Model a behavioral Architecture **Behave** for this 3-bit register.