Name: **Id#**

COE 405, Term 181

Design & Modeling of Digital Systems

Quiz# 1 Solution

Date: Thursday, Sep. 20, 2018

Q.1. Area and testability are two important design criteria that are targeted during design. Explain the importance of minimizing area and having a design testable.

Optimizing area results in lowering the manufacturing cost, increases the manufacturing yields and reduces the packaging cost.

It is important to have a design testable so that manufacturing defects can be detected as early as possible before putting a chip in a system that is sent to the customer. The cost increases by a factor of 10x if a defective part goes from one level to the next without being detected.

Q.2. Performance and power are two important design criteria that are targeted during design. Explain how performance and power of a design are optimized.

Performance is optimized by reducing the critical path in combinational circuits and hence reducing the cycle time.

Power is optimized by reducing the switching activity in a design. It can be also reduced by using a lower voltage and lower clock frequency.

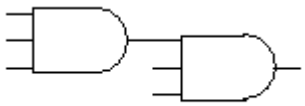
Q.3. Give two examples of semicustom design approaches.

Examples of semicustom design approaches include

- Gate Arrays
  - Mask Programmable (MPGAs)
  - Field Programmable (FPGAs))
- Standard Cells
- Silicon Compilers & Parametrizable Modules (adder, multiplier, memories)

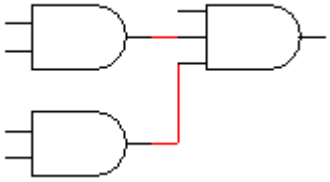
Q.4. Consider the function $F = ABCDE$ and the set of implementations given below. Assume that the area and delay of a gate are directly related to the number of its inputs. Using only 2-input and 3-input AND gates:

(i) Design a circuit to implement the function F with the minimum area. Report the area and delay of your suggested circuit.



Area=6, Delay=6

(ii) Design a circuit to implement the function F with the minimum delay. Report the area and delay of your suggested circuit.



Area=7, Delay=5

Q.5. Consider the function: $F(A,B,C,D) = (A \oplus B)(C \oplus D)$

(i) Compute the expansion of F using the **Orthonormal Basis** $\{\varnothing_1 = \overline{A}\,\overline{B}, \varnothing_2 = \overline{A}B, \varnothing_3 = A\overline{B}, \varnothing_4 = AB\}$.

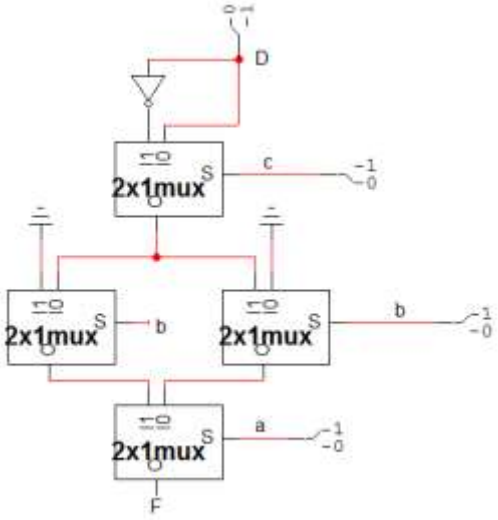
F = A'B' [0] + A'B [C⊕D] + AB' [C⊕D] + AB[0]

(ii) Compute the function $\overline{F}$ utilizing the orthonormal based expansion of the function.

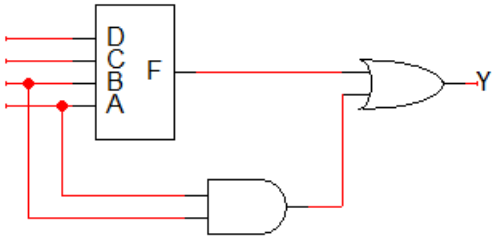
F' = A'B' [1] + A'B [C⊕D]' + AB' [C⊕D]' + AB[1]
= (A⊕B)' + (C⊕D)'(A⊕B)= (A⊕B)' + (C⊕D)'

(iii) Implement the function F using <u>minimal</u> number of 2x1 MUXs and inverters.

F = A' [B' [0] + B [C⊕D]] + A [B' [C⊕D] + B[0]]



(iv) Suppose that the function F is part of a circuit whose output is Y as shown below. Simplify the equation of F to minimum area.



We simply the function using A B as a don't care condition.

	00	01	11	10
00	0 0	0 1	0 3	0 2
01	0 4	1 5	0 7	1 6
11	?12	?13	?15	?14
10	0 8	1 9	011	110

F = B C' D + B C D' + A C' D + A C D' = (A+B)(C⊕D)