Name: KEY **Id#**

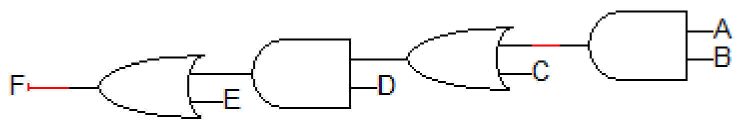
COE 405, Term 152

Design & Modeling of Digital Systems

Quiz# 1

Date: Thursday, Feb. 11, 2016

Q.1. Assume that the area and delay of a gate is related to the number of its inputs i.e., a 2-input AND gate has an area and delay = 2. Consider the given circuit below implementing the function F:



(i) Determine the area and maximum delay of this circuit.

Area = 8, Maximum Delay = 8

(ii) Provide an implementation of this function with an improved delay and determine its area and maximum delay.

F = E + D (C + A B) = E + D C + D A B
Area = 8, Maximum Delay = 6

Q.2. Consider the function: $F(A,B,C,D) = AB + \overline{A}BC + BCD + \overline{A}\overline{D}$

(i) Compute the expansion of F using the **Orthonormal Basis** $\{\varnothing_1 = \overline{A}\overline{B}, \varnothing_2 = \overline{A}B, \varnothing_3 = A\overline{B}, \varnothing_4 = AB\}$.

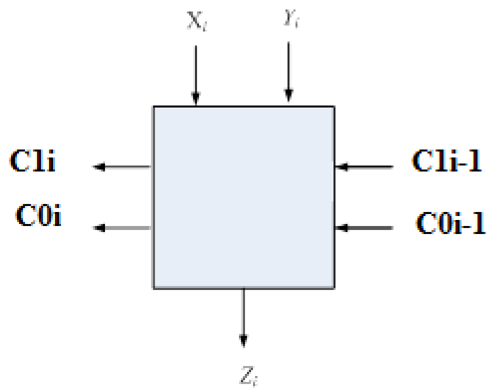
F = A'B' (D') + A'B (C+D') + AB' (0) + AB (1)

(ii) Compute the function $\overline{F}$ utilizing the orthonormal based expansion of the function.

F' = A'B' (D) + A'B (C' D) + AB' (1) + AB (0)
= A'B' D + A'B C' D + AB' = A'B' D + A' C' D + AB'

Q.3. It is required to design a combinational circuit that computes the equation $Z=2X + Y - 1$, where X and Y are n-bit signed 2's complement numbers.

(i) Design the circuit as a modular iterative circuit where each module receives a single bit of the inputs, X_i and Y_i.



(ii) Derive the truth table of your 1-bit module in (i).

$C1_{i-1}$	$C0_{i-1}$	X_i	Y_i	$C1_i$	$C0_i$	Z_i
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	1
0	0	1	1	1	0	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	1	0	0
0	1	1	1	1	0	1
1	0	0	0	0	1	1
1	0	0	1	1	0	0
1	0	1	0	1	0	1
1	0	1	1	1	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	1
1	1	1	0	1	1	0
1	1	1	1	1	1	1