Name: Key **Id#**

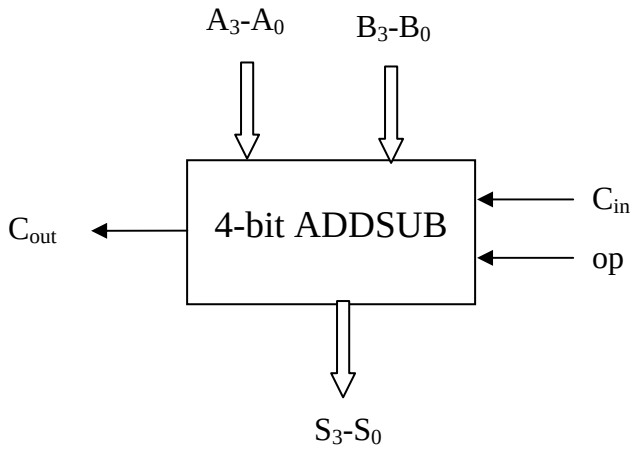
COE 405, Term 021

Design & Modeling of Digital Systems

Quiz# 1

Date: Monday, October 7, 2002

Q.1. It is required to model a 4-bit adder/subtractor. The interface description of the 4-bit adder/substractor is shown below, where **op** determines the operation. When op=0, the operation A+B is performed, otherwise A-B is performed.



(i) Describe an Entity **FAS** for a 1-bit full adder/subtractor.

(ii) Model an Architecture **Conc** for this 1-bit FAS using concurrent statements.

(iii) Describe an Entity **AS4** for a 4-bit adder/subtractor using the interface names given above.

(iv) Model Architecture **Struct** for the 4-bit adder/subtractor (**AS4**) using instantiations of the Entity **FAS**.

(i)

```
Entity FAS IS
        port (A, B, Cin, OP: IN BIT; Sum, Carry: OUT BIT);
END FAS;
```

(ii)

```
Architecture concurrent of FAS IS
signal t: BIT;
Begin
        t      <= b xor op;
        sum    <= a xor t xor cin;
        carry  <= (a and t) or (a and cin) or (t and cin);
End concurrent;
```

(iii)

```
Entity FAS4 IS
      port (A, B: IN Bit_vector(3 downto 0); cin, op: IN bit;
      sum: OUT bit_vector(3 downto 0); cout: OUT BIT);
End FAS4;
```

(iv)

```
Architecture structural of FAS4 IS
signal c0, c1, c2: bit;
component FAS
  port (A, B, Cin, OP: IN BIT; Sum, Carry: OUT BIT);
End Component;
Begin
      b0: FAS port map (A(0), b(0), cin, op, sum(0), c0);
      b1: FAS port map (A(1), b(1), c0, op, sum(1), c1);
      b2: FAS port map (A(2), b(2), c1, op, sum(2), c2);
      b3: FAS port map (A(3), b(3), c2, op, sum(3), cout);
End structural;
```