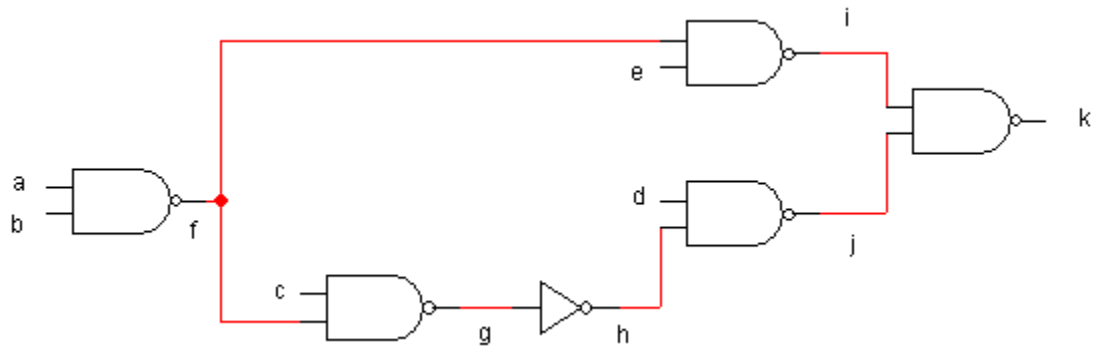
COE 405, Term 152

Design & Modeling of Digital Systems

HW# 7

Due date: Sunday, May 1

Q.1. Consider the logic network below with inputs *{a, b, c, d, e}* and output *{k}*:



Assume that the delay of the inverter gate is 1 and that the delay of the 2-input NAND gate is 2. Also, assume that the input data-ready times are zero except for input *a*, which is equal to 2.

(i) Compute the data ready times and slacks for all vertices in the network.

(ii) Determine the topological critical path.

(iii) Suggest an implementation of the function *k* using only inverters and 2-input NAND gates to reduce the delay of the circuit to the minimum possible and determine the maximum propagation delay in the optimized circuit. Has the area been affected?

Q.2. It is required to design a circuit to compute the equation Y=A+B-C-D, where A, B, C and D are N-bit inputs. Assume that inputs are available only during the first cycle when a **START** input is asserted. Assume that a **DONE** signal will be set when the result is ready and the result will remain held until the next Start operation.

(i) Show a schedule of the operations with minimum latency (i.e., clock cycles) assuming that the clock cycle is limited by the time for performing one addition/subtraction operation. Store the output Y in a register.

(ii) Show the Data Path design of your circuit indicating all the control signals and the used adder/subtractor sizes.

(iii) Show the ASMD diagram of your control unit.

(iv) Write the necessary Verilog modules to module the data path unit, control unit and the overall circuit.

(v) Write a test bench to test the correct operation of your circuit. Include simulation snapshots.

(vi) Implement your circuit on FPGA assuming N=2 bits. Include a link for a video snapshot to demonstrate correct functionality of your circuit.

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a ***word file*** *that contains the following items:*

i. Your name and ID

ii. Assignment number

iii. Problem statement

iv. Your solution

v. Include snapshots of simulation output to illustrate the correctness of your models.