COE 405, Term 152

Design & Modeling of Digital Systems

HW# 5

Due date: Thursday, April 7

Q.1. It is required to design a circuit that receives two **4-bit** signed numbers in 2's complement representation $\mathbf{A=A_3A_2A_1A_0}$, $\mathbf{B=B_3B_2B_1B_0}$ and produces **5-bit output** $\mathbf{C= C_4C_3C_2C_1C_0}$. The circuit implements the following functions based on the values of the three selection inputs: S1, S1 and S0.

S2 S1 S0	Function
0 0 0	C = A + B
0 0 1	C = A - B
0 1 0	C = A + 1
0 1 1	C = A + 2
1 0 0	C = A - 1
1 0 1	C = A - 2
1 1 0	C = 2A
1 1 1	C = 2B

(i) Show the block diagram design of your circuit using MSI components like Adder, Multiplexor, as needed. Use only one adder in your solution.

(ii) Model your design in Verilog by modeling each component separately i.e. adder, MUX, etc. and then instantiating these components to model your circuit.

(iii) Write a Verilog test bench to test your design and verify its correctness by simulation. For each function, test at least 2 input combinations of your choice to demonstrate correct functionality. Show snapshots of your simulation to demonstrate its correctness.

(iv) Write another Verilog model that models the circuit behaviorally. Make your model parametrizable where n is the inputs width in bits.

(v) Use the test bench you developed in (iii) to test the correctness of your behavioral model. Show snapshots of your simulation to demonstrate its correctness.

(vi) Implement your behavioral model on FPGA and demonstrate its correct functionality for n=2. Include a link for a video snapshot to demonstrate correct functionality of your circuit on FPGA.

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a ***word file*** *that contains the following items:*

i. *Your name and ID*

ii. *Assignment number*

iii. *Problem statement*

iv. *Your solution*

v. Include snapshots of simulation output to illustrate the correctness of your models.