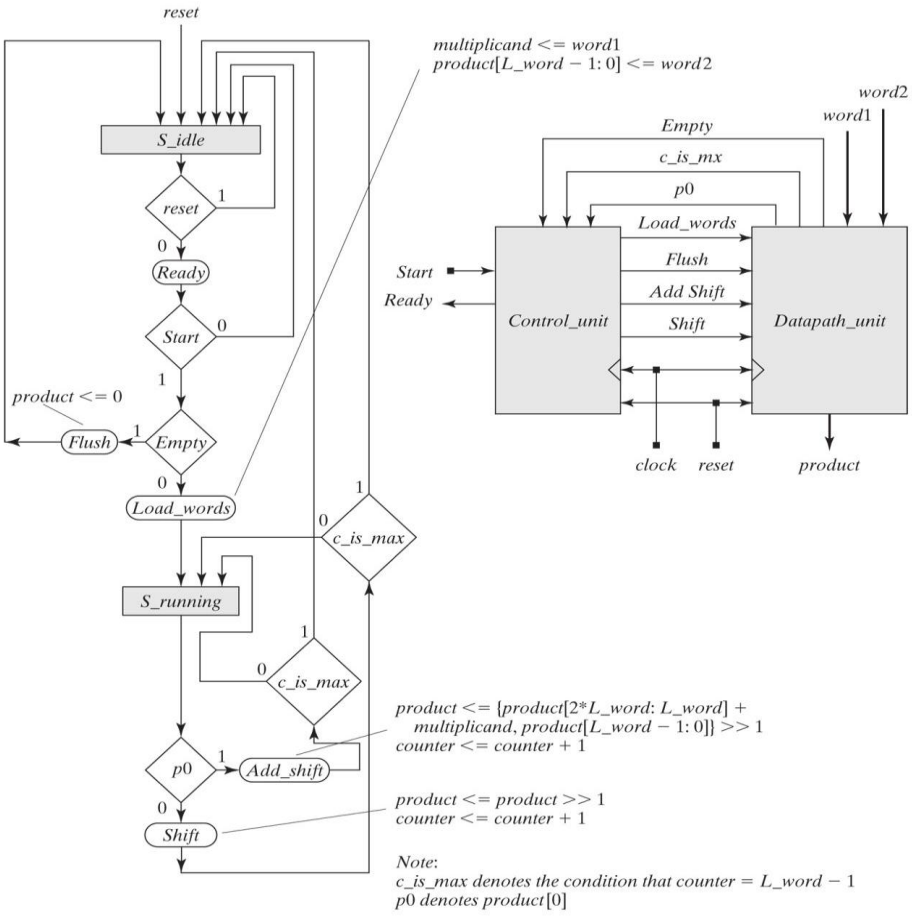
COE 405, Term 122

Design & Modeling of Digital Systems

HW# 5

Due date: Monday, April 15

Q.1. It is required to design an unsigned 4-bit sequential multiplier. The multiplier is assumed to have an 8-bit register to hold the result, a 4-bit register to hold the multiplicand and a 3-bit counter. When reset is 1, the multiplicand, the product and counter registers are reset. When operation is started, the multiplicand register is loaded with word1 while the least significant 4-bits of the product are loaded with word2. The block diagram and the ASMD chart of the sequential multiplier are given below. *Ready* signals that the unit is ready to accept a command to multiply. If word1 or word2 are 0, *Empty* is set to 1. *Flush* loads the product with 0. *C_is_mx* is set when the counter is equal to 3. *P0* is the least significant bit of the product i.e. product[0].



(i) Write a Verilog model to model the data-path.

(ii) Write a Verilog model to model the control unit based on the ASMD chart i.e. not based on equations.

(iii) Write a Verilog test bench to test the correctness of a 4-bit sequential multiplier.

(iv) Implement the 4-bit sequential multiplier using FPGA and demonstrate its correctness.