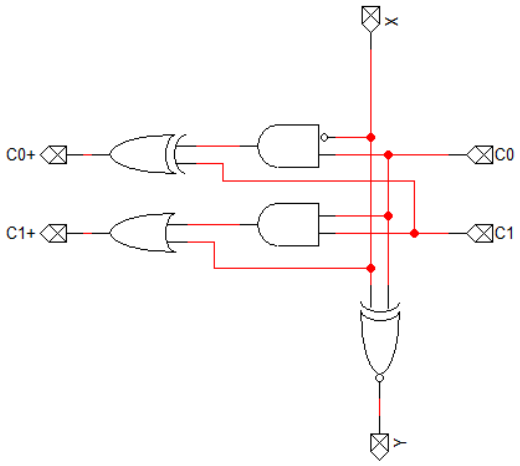
COE 405, Term 152

Design & Modeling of Digital Systems

HW# 4

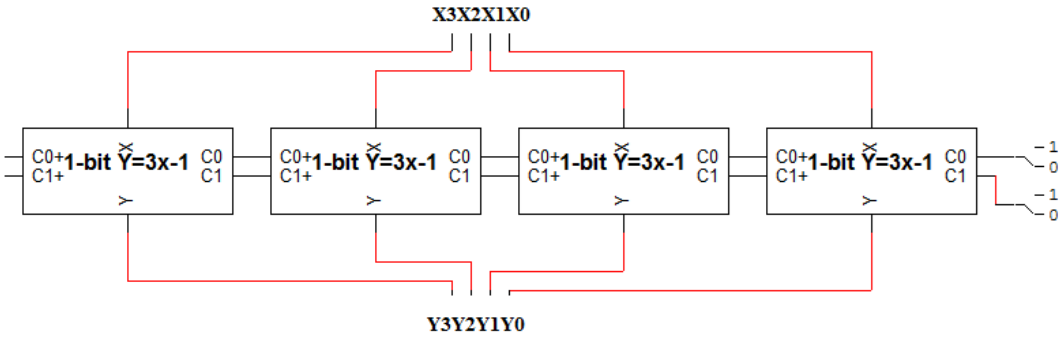
Due date: Tuesday, March 22

Q.1. An iterative design of a combinational circuit that computes the equation Y=3*X-1, where X is an n-bit signed 2's complement number is given below:



(i) Write a Verilog model to model the given 1-bit cell using primitive gates. Model the delay of AND and OR gates as 5ps, while the delay of XOR and XNOR gates as 8 ps.

(ii) Write a Verilog model for modeling the circuit given below computing the equation Y=3*X-1 assuming X is a 4-bit number by instantiating 4 cells:



(iii) Write a test bench to test the correctness of your Verilog model by applying the following input patterns $X_3X_2X_1X_0$={0000, 0001, 0011, 0101, 1111, 1110}. Apply consecutive inputs patterns after a delay of 20ps.

(iv) Determine the longest delay of your 4-bit circuit.

(v) Write a test bench to verify the longest delay of your 4-bit circuit.

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a ***word file*** *that contains the following items:*

i. Your name and ID

ii. Assignment number

iii. Problem statement

iv. Your solution

v. Include snapshots of simulation output to illustrate the correctness of your models.