COE 405, Term 031

Design & Modeling of Digital Systems

HW# 4

Due date: Sunday, Nov. 30, 2003

Q.1. 5.15

Q.2. 5.17

Q.3. 5.20

Q.4. Modify the design of the array multiplier that you have modeled in HW#3 to make it a pipelined multiplier. Use the necessary number of pipeline stages to make the speed of your multiplier limited by the speed of the adder. Simulate your design and verify that it is working properly.