COE 405, Term 152

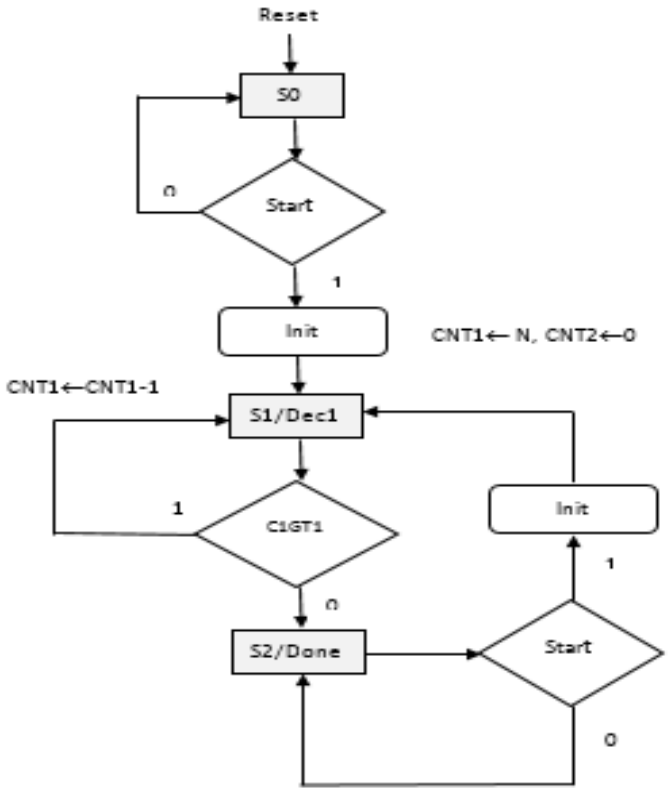
Design & Modeling of Digital Systems

HW# 3 Solution

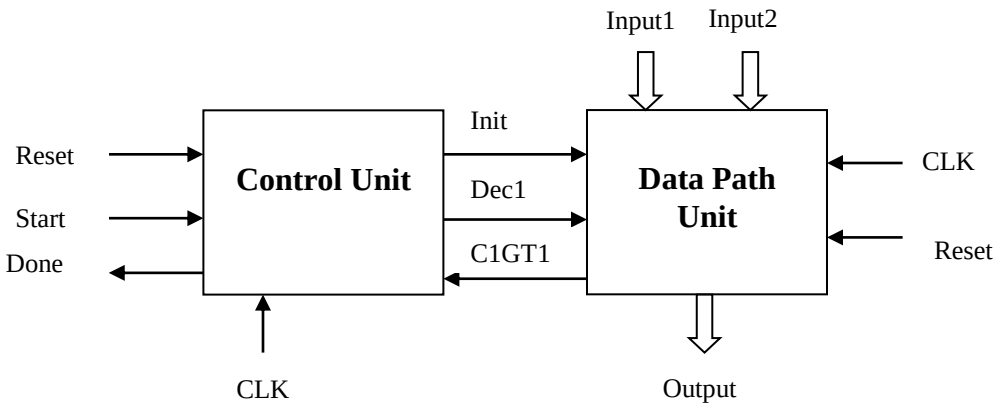
Due date: Tuesday, March 1

Q.1. It is required to design a circuit that receives an array of n unsigned 4-bit numbers along with a 4-bit target value and counts the number of data elements that are greater or equal to the target value. Assume that once the user presses *Start* he will also supply the number of elements in the array n ($n \leq 15$) through input1 and the target value through input2 in the same cycle. Assume that input2 will hold the target value until the circuit finishes its operation. In the next n consecutive cycles, the user will provide the n data elements through input1. Once the circuit finishes computation, it will assert a *Done* signal and will generate a 4-bit output indicating the count of the number of elements in the array ≥ target value. The *Done* signal and the result will remain valid unless the user resets the machine or asserts the *Start* signal.

(i) Develop an ASMD chart for the circuit.

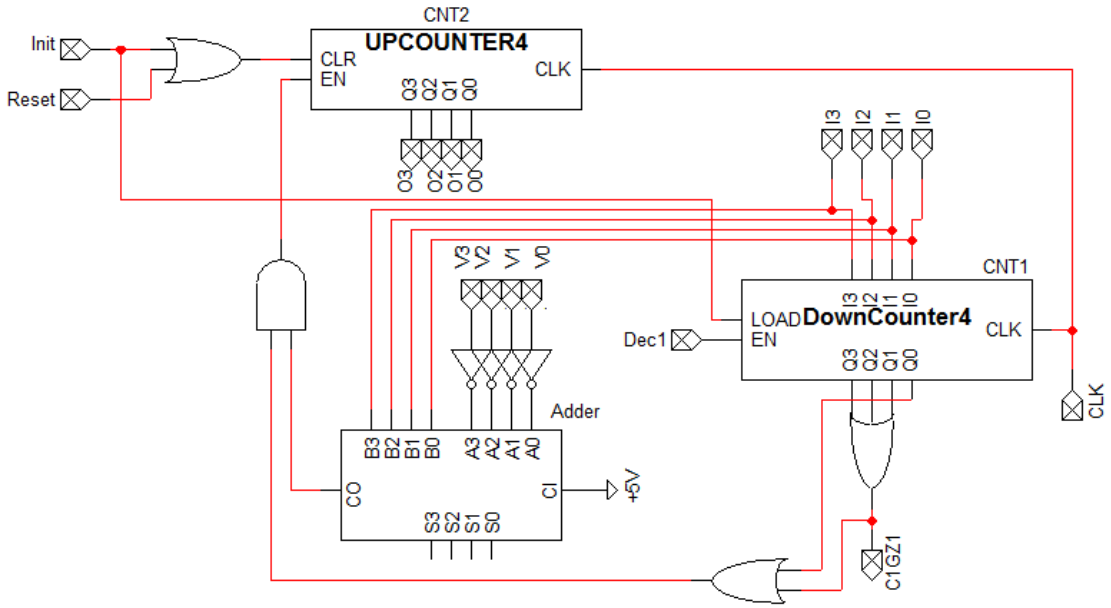


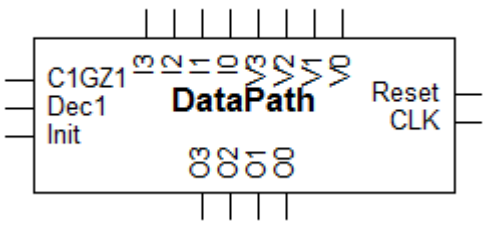
(ii) Show a block diagram for the datapath and control unit interface.



(iii) Show the design of the data-path and control unit of the circuit.

Data Path:





Control Unit:

C.S.	Input		N.S.	Output		
	Start	C1GZ1		Init	Dec1	Done
S0	0	X	S0	0	0	0
S0	1	X	S1	1	0	0
S1	x	0	S2	0	1	0
S1	x	1	S1	0	1	0
S2	0	X	S2	0	0	1
S2	1	X	S1	1	0	1

We use the binary state assignment S0=00, S1=01, S2=10, and the two Flip Flops, F1 F0, to encode states.

The output signals equations are as follows:

Init = F0' Start

Dec1 = F0

Done = F1

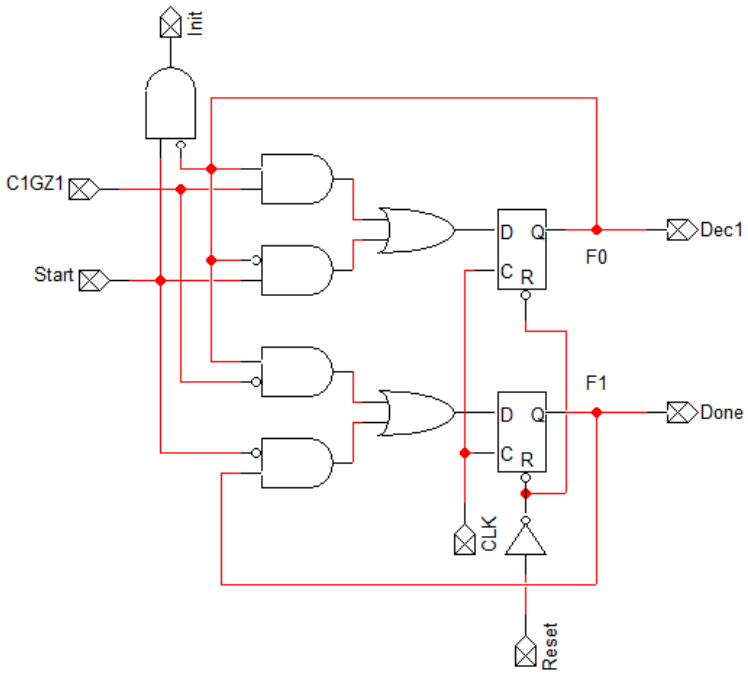
The next state equations are as follows:

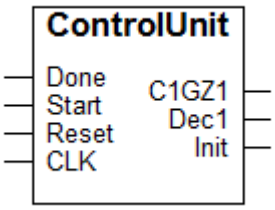
	00	01	11	10
00	0 0	0 1	1 3	1 2
01	0 4	1 5	1 7	0 6
11	? 12	? 13	? 15	? 14
10	0 8	0 9	1 11	1 10

F0+= F0 C1GZ1 + F0' Start

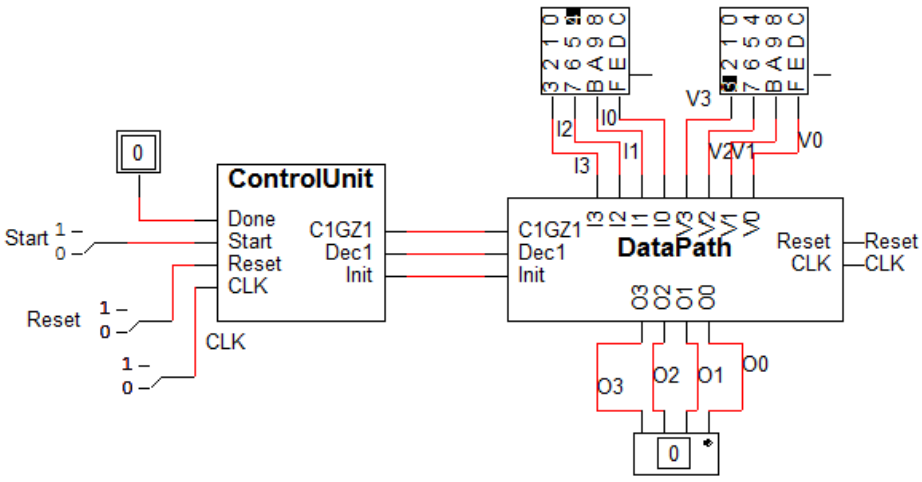
	00	01	11	10
00	0 0	0 1	0 3	0 2
01	1 4	0 5	0 7	1 6
11	? 12	? 13	? 15	? 14
10	1 8	1 9	0 11	0 10

F1+ = F0 C1GZ1' + F1 Start'

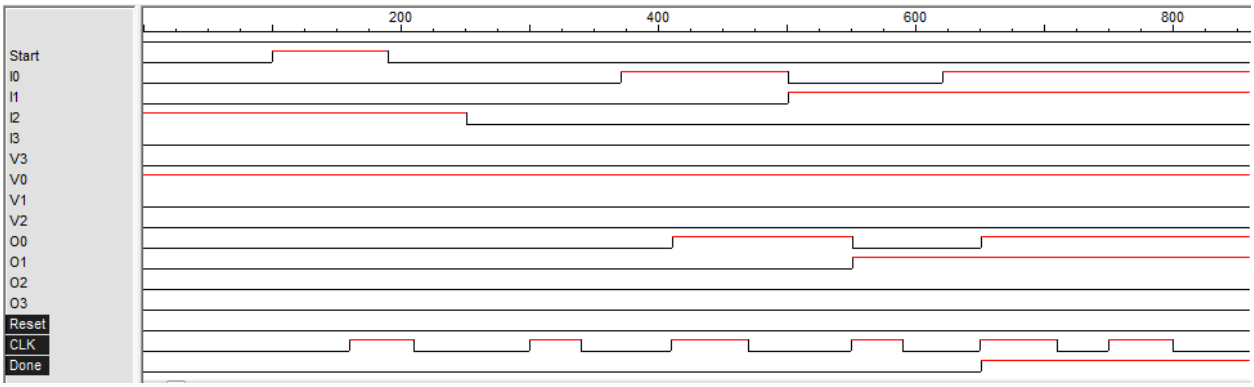




(iv) Implement the circuit using logicworks and verify its correct functionality by simulation.



The correctness of the circuit is demonstrated in the timing diagram below where when Start is asserted the number of data values=4 is entered. The target value is set as 1. Then the values 0, 1, 2, and 3 are entered. We can see that the resulting output value is 3, which is the correct value.



The timing diagram of another example is shown below which demonstrates that when Start is asserted, the number of data values=5 is entered. The target value is set as 4. Then the values 1, 2, 3, 4, and 5 are entered in subsequent cycles. We can see that the resulting output value is 2, which is the correct value.