COE 405, Term 062

Design & Modeling of Digital Systems

HW# 3

Due date: Monday, April 16, 2007

Q.1. You are required to model an ALU that has the following entity description:

```
Entity ALU is
        Generic (N: Natural :=4);
        Port (A, B: IN Bit_Vector(N-1 Downto 0);
            Cin: IN Bit;
            Sel: IN Bit_Vector(2 Downto 0);
            C: OUT Bit_Vector(N-1 Downto 0);
            Cout, SignF, OverflowF, ZeroF: OUT BIT
            );
End;
```

The ALU performs one of eight different functions according to selection line inputs as shown in the table given below:

Sel	Function
000	**C=A+B**
001	**C=A+B+Cin**
010	**C=A-B**
011	**C=A-B-Cin**
100	**C=B+1**
101	**C=B-1**
110	**C=B**
111	**C=2*B**

The four flags Cout, SignF, OverflowF and ZeroF are computed according to the result. Note that the Cout flag is considered a borrow when a subtraction operation is performed.

(i) Model the following two functions, "+" and "-", to support addition and subtraction on Bit_Vector. Model the functions by converting Bit_Vector type to Integer, perform the required operation in integer and then convert the result back to Bit_Vector type. Assume that the returned result has length one extra bit more than the inputs to return the carry out.

Function "+" (l, r : Bit_Vector) RETURN Bit_vector IS

Function "-" (l, r : Bit_Vector) RETURN Bit_vector IS

(ii) Write a behavioral model for modeling the ALU using the developed functions in (i).

(iii) Write a test bench for testing the n-bit ALU assuming that the input arguments are read from an input file and that the output will be stored in an output file. Use TEXTIO package for this purpose. Apply the following values for testing the correct operation of a 4-bit ALU:

ALU Select	Input A	Input B	Cin
000	5	2	
000	-8	7	
000	7	7	
000	-7	-2	
000	-1	1	
000	-1	-1	
001	-1	1	1
001	-1	-1	0
001	-1	-1	1
001	-1	0	1
010	3	4	
010	-8	7	
010	-7	-1	
010	-7	2	
011	-7	1	1
011	3	2	1
011	-8	1	1
100		-1	
100		1	
100		7	
101		0	
101		-1	
101		-8	
101		7	
110		-1	
110		7	
111		-1	
111		3	
111		7	

The output should be stored in the output file using the following format:

ALU Operation	Input A	Input B	Result	Cout	Signf	OverflowF	ZeroF
C=A+B	5	2	7	0	0	0	0

(iv) Define a package called HW3 where you store all used types, subtypes, functions and procedures inside the package and use the package when needed.

(v) Synthesize the modeled ALU in (ii) using Xilinx Project Navigator and report on the total equivalent gate count for design after mapping and the longest delay in the design based on Post-Map static timing report.

(vi) Remodel the functions in (i), "+" and "-", based on performing the operation using a ripple carry add like functionality. Change the ALU model based on the use of these two newly modeled functions and reapply the same test bench modeled in (iii) to verify the correct functionality of the ALU.

(vii) Synthesize the modeled ALU in (vi) using Xilinx Project Navigator and report on the total equivalent gate count for design after mapping and the longest delay in the design based on Post-Map static timing report. Compare the gate count and maximum delay obtained with that obtained in (v). What are your observations and conclusions?

(viii) Remodel the functions in (i), "+" and "-", based on performing the operation using a cascaded 4-bit carry-look-ahead like functionality. Change the ALU model based on the use of these two newly modeled functions and reapply the same test bench modeled in (iii) to verify the correct functionality of the ALU.

(ix) Synthesize the modeled ALU in (viii) using Xilinx Project Navigator and report on the total equivalent gate count for design after mapping and the longest delay in the design based on Post-Map static timing report. Compare the gate count and maximum delay obtained with that obtained in (vii). What are your observations and conclusions?