COE 405, Term 031

Design & Modeling of Digital Systems

HW# 3

Due date: Sunday, Nov. 9, 2003

Q.1. It is required to model in VHDL a parametrizable **n-bit *Ripple Carry Adder***.

(i) Describe the entity of the n-bit adder using GNERIC for passing the adder size.

(ii) Model architecture for the n-bit adder using GENERATE statement.

(iii) Define a package called HW3 where you store all used components, functions and procedures inside the package and use the package when needed.

(iv) Write a test bench for testing the n-bit ripple carry adder assuming that the input arguments will be specified using the procedure Apply_Data given in the book..

(v) Write a test bench for testing the n-bit ripple carry adder assuming that the input arguments will be read as integers from an input file and that the output will be stored as integer in an output file. Use TEXTIO package for this purpose. **Hint**: assignments scheduled on signals inside a process take effect after encountering a wait statement. Use the statement **wait for 0 ns** as many times as needed for this purpose.

Q.2. It is required to model in VHDL a parametrizable **n-bit *Array Multiplier***.

(i) Describe the entity of the n-bit array multiplier using GNERIC for passing the adder size. Note that while the multiplier inputs are n-bits each, the multiplier output is 2n bits.

(ii) Model architecture for the n-bit array multiplier using GENERATE statement. Use the n-bit ripple carry adder modeled in Q1 in your solution.

(iii) Modify the test bench developed for the adder in Q1(v) to test the n-bit multiplier. Assume that the input arguments will be read as integers from an input file and that the output will be stored as integer in an output file. Use TEXTIO package for this purpose.