COE 405, Term 152

Design & Modeling of Digital Systems

HW# 2 Solution

Due date: Thursday, Feb. 25

Q.1. It is required to design a sequential circuit that has a single input X representing a signed 2's complement number and a single output Y. The circuit receives the number serially through the input X from the least significant bit (LSB) to the most significant bit (MSB), and computes the equation Y=3*X-2 and generates the output serially from the least significant bit to the most significant bit. The circuit has an additional asynchronous reset input R that resets the circuit into an initial state. The following are examples of input and output data:

Examples:

		LSB				MSB	
Input	X	0	1	1	0	0	Input=6
Output	Y	0	0	0	0	1	Output=16

		LSB				MSB	
Input	X	1	1	0	0	0	Input=3
Output	Y	1	1	1	0	0	Output=7

(i) Draw the state diagram of the circuit assuming a **Mealy** model.

Present State	**Next State, Y**	
	X=0	**X=1**
S0 (B=2)	S1, 0	S2, 1
S1 (B=1)	S1, 1	S3, 0
S2 (B=0)	S2, 0	S3, 1
S3 (C=1)	S2, 1	S4, 0
S4 (C=2)	S3, 0	S4, 1

(ii) Implement the circuit using D-FFs.

Since we have 5 states, we need 3 FFs: F2, F1, and F0. We will use the following encoding: S0=000, S1=001, S2=010, S3=011, S4=100.

Present State F2F1F0	Next State, Y	
	X=0	X=1
0 0 0	0 0 1, 0	0 1 0, 1
0 0 1	0 0 1, 1	0 1 1, 0
0 1 0	0 1 0, 0	0 1 1, 1
0 1 1	0 1 0, 1	1 0 0, 0
1 0 0	0 1 1, 0	1 0 0, 1

	00	01	11	10
00	0 0	1 1	0 3	1 2
01	0 4	1 5	0 7	1 6
11	? 12	? 13	? 15	? 14
10	0 8	1 9	? 11	? 10

Y = F0' X + F0 X' = F0 ⊕ X

	00	01	11	10
00	1 0	0 1	1 3	1 2
01	0 4	1 5	0 7	0 6
11	? 12	? 13	? 15	? 14
10	1 8	0 9	? 11	? 10

F0+ = F1' F0 + F1' X' + F1 F0' X = F1' (F0 + X') + F1 F0' X = F1 ⊕ (F0 + X')

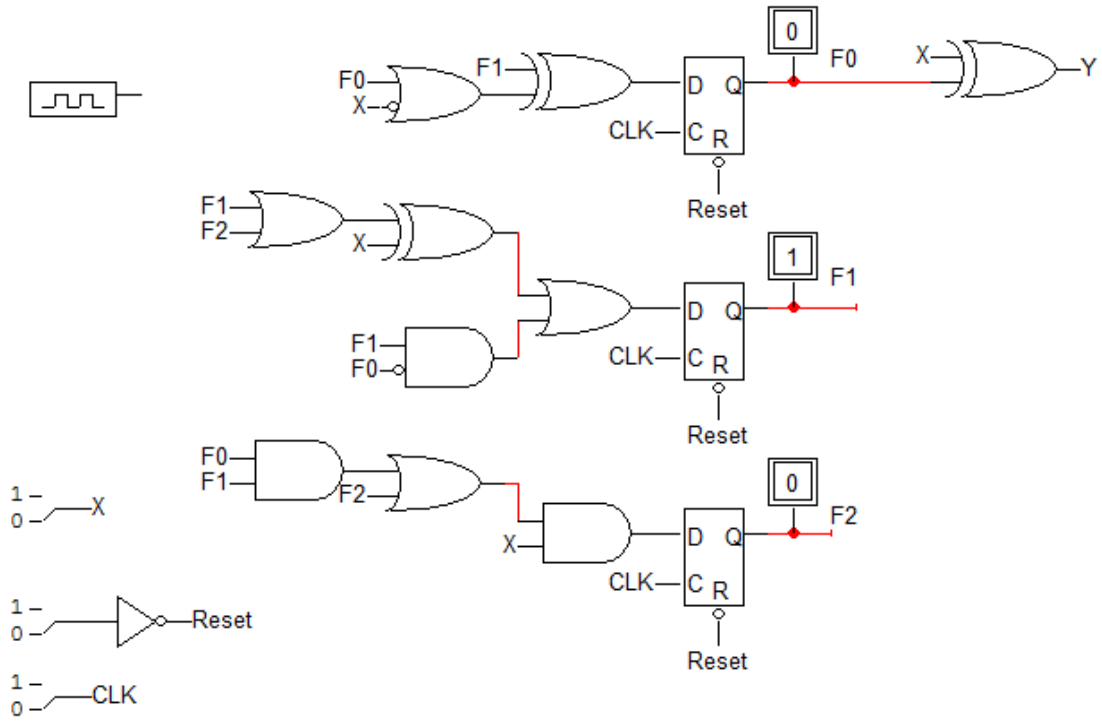
	00	01	11	10
00	0 0	1 1	1 3	0 2
01	1 4	1 5	0 7	1 6
11	? 12	? 13	? 15	? 14
10	1 8	0 9	? 11	? 10

F1+ = F2'F1' X + F1 F0' + F1 X' + F2 X' = F2'F1' X + X' (F1 + F2) + F1 F0' = X ⊕ (F1 + F2) + F1 F0'

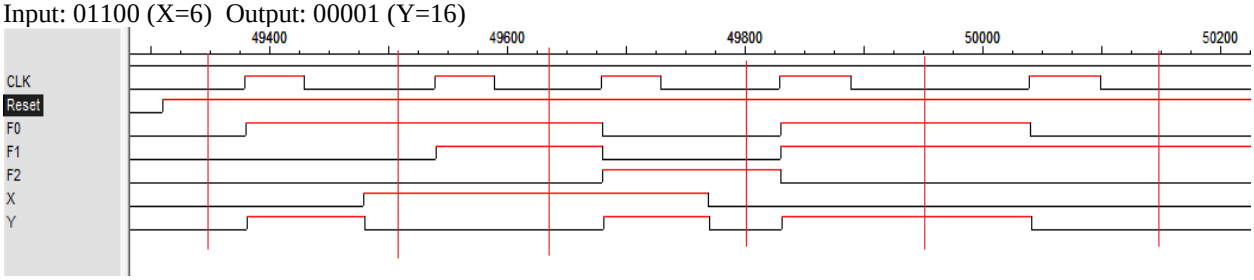
	00	01	11	10
00	0 0	0 1	0 3	0 2
01	0 4	0 5	1 7	0 6
11	? 12	? 13	? 15	? 14
10	0 8	1 9	? 11	? 10

F2+ = F2 X + F1 F0 X = X (F2 + F1 F0)

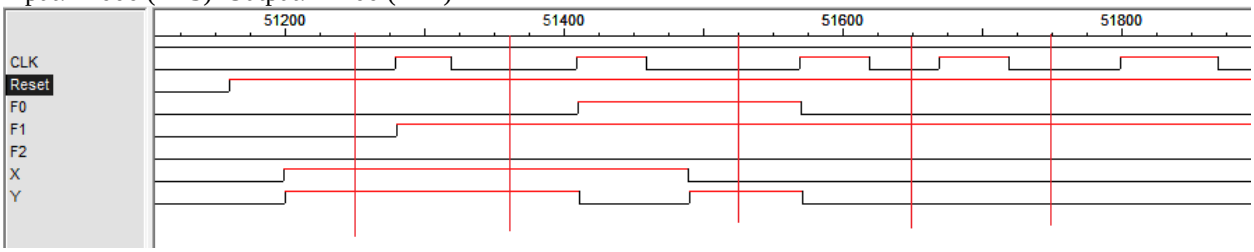
(iii) Verify the correctness of your circuit by simulation.



Input: 01100 (X=6) Output: 00001 (Y=16)



Input: 11000 (X=3) Output: 11100 (Y=7)



Q.2. Consider the given FSM that has 6 states, two inputs X and Y, and one output Z, represented by the following state table:

Present State	**Next State**				**Output**
	XY=00	**XY=01**	**XY=10**	**XY=11**	**Z**
S0	S0	S1	S2	S3	1
S1	S0	S3	S1	S4	0
S2	S1	S3	S2	S4	1
S3	S1	S0	S4	S5	0
S4	S0	S1	S2	S5	1
S5	S1	S4	S0	S5	0

(i) Determine the equivalent states.

S1					
S2	(0,1), (1,3), (3,4)				
S3		(0,1), (0,3), (1,4), (4,5)			
S4	(3,5)		(0,1), (1,3), (4,5)		
S5		(0,1), (3,4), (4,5)		(0.4)	
	S0	S1	S2	S3	S4

Thus, the equivalent states are (S0, S4) and (S3, S5).

(ii) Reduce the state table into the minimum number of states and show the reduced state table.

The reduced state table is as follows:

Present State	**Next State**				**Output**
	XY=00	**XY=01**	**XY=10**	**XY=11**	**Z**
S0	S0	S1	S2	S3	1
S1	S0	S3	S1	S0	0
S2	S1	S3	S2	S0	1
S3	S1	S0	S0	S3	0

Q.3. Consider the given FSM that has 4 states, one input (X) and one output (Z), represented by the following state table:

Present State	**Next State, Z**	
	X=0	**X=1**
S0	S0, 1	S2, 0
S1	S0, 0	S2, 0
S2	S1, 0	S3, 0
S3	S1, 0	S3, 1

(i) Implement the FSM using the following state assignment: S0=00, S1=01, S2=10, S3=11.

	00	**01**	**11**	**10**
0	1 0	0 1	0 3	0 2
1	0 4	0 5	1 7	0 6

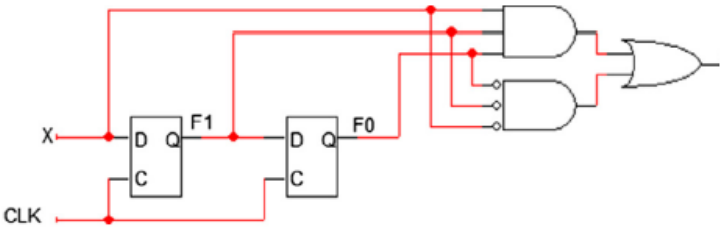
Y = F1' F0' X' + F1 F0 X

	00	01	11	10
0	0 0	0 1	0 3	0 2
1	1 4	1 5	1 7	1 6

F0+ = F1

	00	01	11	10
0	0 0	1 1	1 3	0 2
1	0 4	1 5	1 7	0 6

F1+= X



(ii) Implement the FSM using the following state assignment: S0=01, S1=10, S2=11, S3=00.

	00	01	11	10
0	0 0	1 1	0 3	1 2
1	0 4	0 5	0 7	0 6

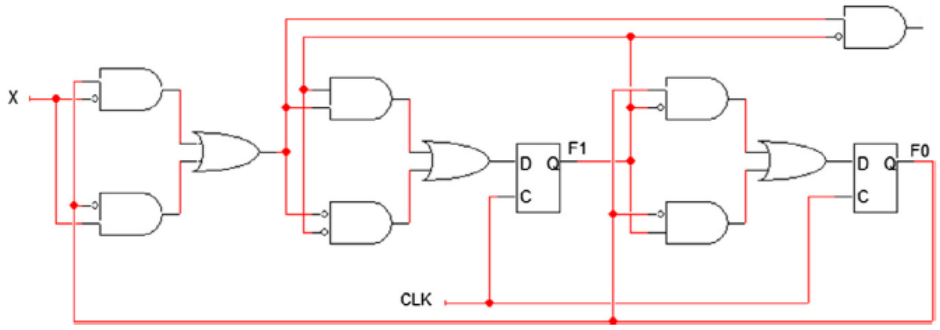
Z = F1' F0' X + F1' F0 X' = F1' (F0' X + F0 X') = F1' (F0 ⊕ X)

	00	01	11	10
0	0 0	0 1	1 3	1 2
1	1 4	1 5	0 7	0 6

F0+ = F1' F0 + F1 F0' = F1 ⊕ F0

	00	01	11	10
0	1 0	0 1	1 3	0 2
1	0 4	1 5	0 7	1 6

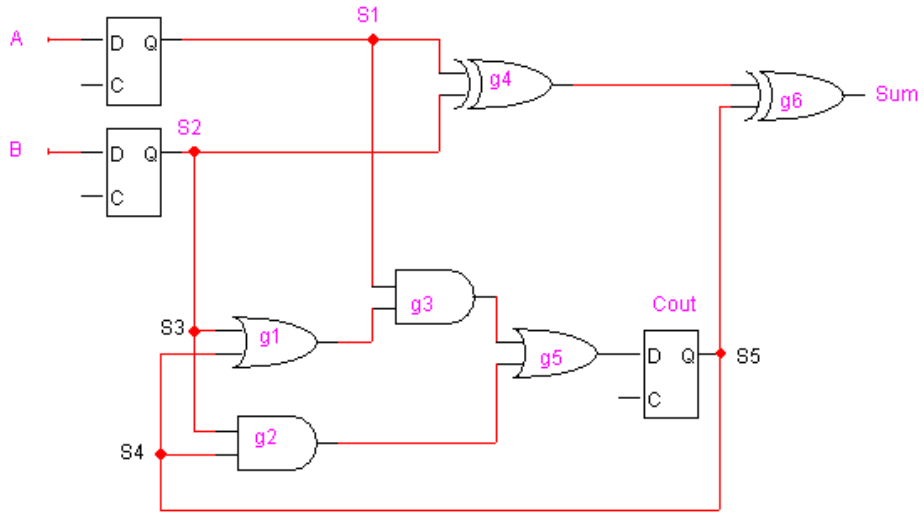
F1+ = F1' F0' X' + F1' F0 X + F1 F0' X + F1 F0 X' = F1' (F0' X' + F0 X) + F1 (F0' X + F0 X')
= F1 ⊕ F0 ⊕ X



(iii) Compare the area of the two resulting circuits.

The number of literals using the first state assignment is 6 while it is 14 using the second state assignment. We could also say that the first assignment uses an equivalent of 5 2-input primitive gates while the second state assignment uses 10 2-input primitive gates. Therefore, the first assignment produces a significantly lower area than the second assignment.

Q.4. Consider the circuit given below representing a serial adder. Assume that the delay of a 2-input AND gate is 2 unit delays, the delay of a 2-input OR gate is 2 unit delays and the delay of a 2-input XOR gate is 4 unit delays.



(i) Determine the critical path of this circuit and the maximum propagation delay.

(i) The critical path is {g4, g6} which is 8 unit delays.

(ii) Using only the **Retiming** transformation, reduce the critical path of this circuit with the minimum number of flip-flops possible.

(ii) The critical path can be reduced to 6 without increasing the number of flip-flops as follows:

- retime s_5 by -1 (i.e. forward retiming)
- retime s_1 by -1
- retime s_2 by -1
- retime g_4 by -1
- retime s_4 by -1
- retime s_3 by -1
- retime g_1 by -1
- retime g_2 by -1
- retime g_3 by -1
- retime g_5 by -1

The resulting circuit after retiming is: