

## COE 405, Term 152

### Design & Modeling of Digital Systems

#### HW# 2

**Due date: Thursday, Feb. 25**

- Q.1.** It is required to design a sequential circuit that has a single input X representing a signed 2's complement number and a single output Y. The circuit receives the number serially through the input X from the least significant bit (LSB) to the most significant bit (MSB), and computes the equation  $Y=3*X-2$  and generates the output serially from the least significant bit to the most significant bit. The circuit has an additional asynchronous reset input R that resets the circuit into an initial state. The following are examples of input and output data:

Examples:

		LSB			MSB		
Input	X	0	1	1	0	0	Input=6 Output=16
Output	Y	0	0	0	0	1	

		LSB			MSB		
Input	X	1	1	0	0	0	Input=3 Output=7
Output	Y	1	1	1	0	0	

- (i) Draw the state diagram of the circuit assuming a **Mealy** model.
  - (ii) Implement the circuit using D-FFs.
  - (iii) Verify the correctness of your circuit by simulation.
- Q.2.** Consider the given FSM that has 6 states, two inputs X and Y, and one output Z, represented by the following state table:

Present State	Next State				Output
	XY=00	XY=01	XY=10	XY=11	Z
S0	S0	S1	S2	S3	1
S1	S0	S3	S1	S4	0
S2	S1	S3	S2	S4	1
S3	S1	S0	S4	S5	0
S4	S0	S1	S2	S5	1
S5	S1	S4	S0	S5	0

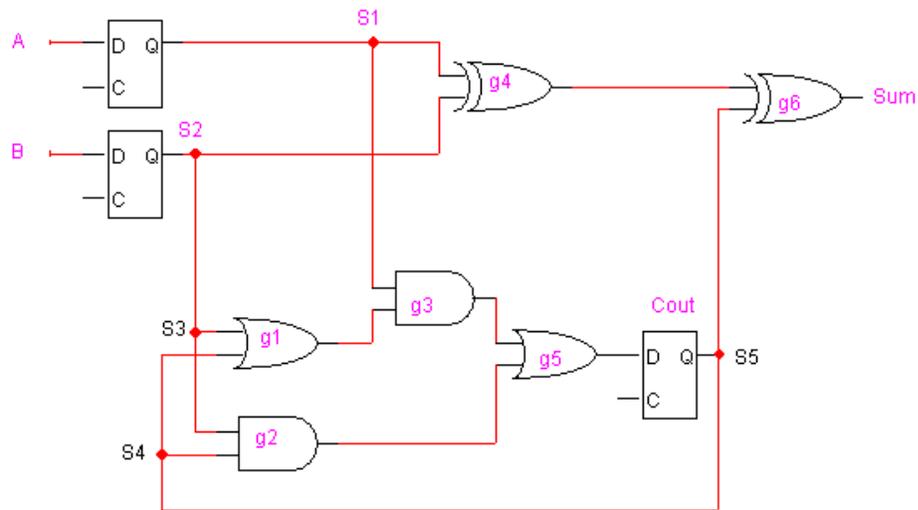
- (i) Determine the equivalent states.
- (ii) Reduce the state table into the minimum number of states and show the reduced state table.

**Q.3.** Consider the given FSM that has 4 states, one input (X) and one output (Z), represented by the following state table:

Present State	Next State, Z	
	X=0	X=1
S0	S0, 1	S2, 0
S1	S0, 0	S2, 0
S2	S1, 0	S3, 0
S3	S1, 0	S3, 1

- (i) Implement the FSM using the following state assignment: S0=00, S1=01, S2=10, S3=11.
- (ii) Implement the FSM using the following state assignment: S0=01, S1=10, S2=11, S3=00.
- (iii) Compare the area of the two resulting circuits.

**Q.4.** Consider the circuit given below representing a serial adder. Assume that the delay of a 2-input AND gate is 2 unit delays, the delay of a 2-input OR gate is 2 unit delays and the delay of a 2-input XOR gate is 4 unit delays.



- (i) Determine the critical path of this circuit and the maximum propagation delay.
- (ii) Using only the **Retiming** transformation, reduce the critical path of this circuit with the minimum number of flip-flops possible.