COE 405, Term 031

Design & Modeling of Digital Systems

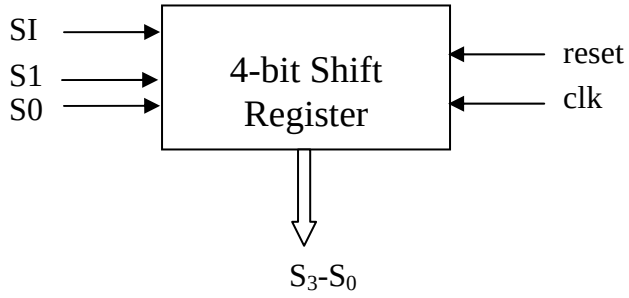
HW# 2

Due date: Sunday, October 26, 2003

Q.1. It is required to design a 4-bit shift register. The shift register should be able to shift or rotate either left or right based on the following table:

S1 S0	Operation
00	Shift left
01	Shift right
10	Rotate left
11	Rotate right

The reset is a synchronous reset and the shift register is rising-edge triggered. Assume that the shifted bit is based on the input SI. The interface description of the 4-bit shifter is shown below.



(i) Describe an Entity **Shifter4** for the 4-bit shift register.

(ii) Model a behavioral Architecture **Behave** for this 4-bit shift register. Verify its correctness by simulation.

(iii) Model a structural Architecture **Struct** for this 4-bit shift register. Verify its correctness by simulation.

Q.2. Problem 4.15.

Have your VHDL code commented; include snapshots of your simulation. Include both hard and soft copy of your solutions. The hard copy should be well organized and include everything required in the questions. The soft copy should be supplied in a floppy disk along with a Readme file describing its content. Both the hard and soft copy should be submitted in a sealed envelope.