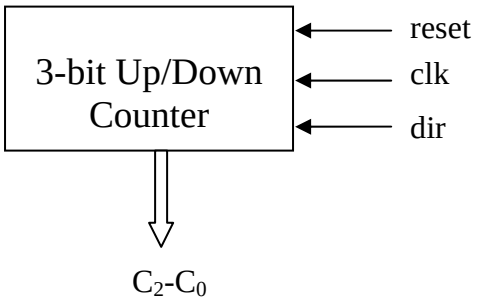
COE 405, Term 021

Design & Modeling of Digital Systems

HW# 2

Due date: Saturday, October 19, 2002

Q.1. It is required to design a 3-bit up/down counter. The interface description of the 3-bit up/down counter is shown below, where **dir** determines the counter operation. When dir=0, the counter will be counting up, otherwise it will be counting down. The reset is a synchronous reset and the counter is rising-edge triggered.

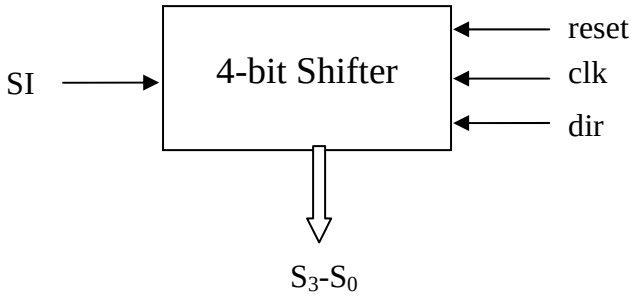


(i) Describe an Entity **Count3** for the 3-bit up/down counter.

(ii) Model a behavioral Architecture **Behave** for this 3-bit up/down counter. Verify its correctness by simulation.

(iii) Model a structural Architecture **Struct** for this 3-bit up/down counter. Verify its correctness by simulation.

Q.2. It is required to design a 4-bit shifter. The shifter should be able to shift either left or right based on a control input **dir**. When dir=0 it shifts left and when dir=1 it shifts right. **SI** is the shift input. The reset is a synchronous reset and the shifter is rising-edge triggered. The interface description of the 4-bit shifter is shown below.



(i) Describe an Entity **Shifter4** for the 4-bit shifter.

(ii) Model a behavioral Architecture **Behave** for this 4-bit shifter. Verify its correctness by simulation.

(iii) Model a structural Architecture **Struct** for this 4-bit shifter. Verify its correctness by simulation.

For both problems, have your VHDL code commented; include snapshots of your simulation. Include both hard and soft copy of your solutions. The hard copy should be well organized and include everything required in the questions. The soft copy should be supplied in a floppy disk along with a Readme file describing its content.
Both the hard and soft copy should be submitted in a sealed envelope.