COE 405, Term 152

Design & Modeling of Digital Systems

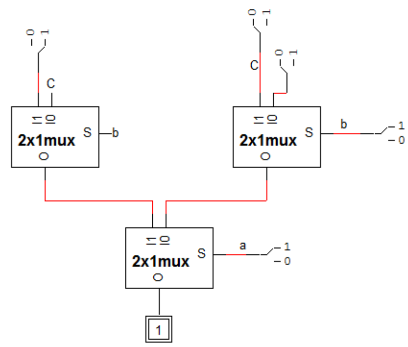
HW# 1 Solution

Due date: Thursday, Feb. 11

Q.1. Consider the two functions f=a ⊕ b ⊕ c and g=a b + a c + b c.

(i) Implement the function g using only 2x1 MUXs.

g = a' [b c] + a [b + c] = a' [b' [0] + b [c]] + a [b'[c] + b[1]]



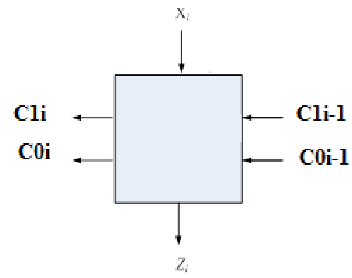
(ii) Compute the function f⊕g based on orthonormal basis expansion.

f = a'b' [c] + a'b [c'] + ab' [c'] + ab [c]
g = a'b' [0] + a'b [c] + ab' [c] + ab [1]
f⊕g = a'b' [c] + a'b [1] + ab' [1] + ab [c'] = a'b'c + a'b + ab' + abc' = a'c + a'b + ab' + ac'

Q.2. It is required to design a combinational circuit that computes the equation Y=3*X-1, where X is an n-bit signed 2's complement number.

(i) Design the circuit as a modular circuit where each module receives a single bit of the input, X_i.

This circuit can be designed by assuming that we have a borrow feeding the first cell or by representing -1 in 2's complement as 11…111 and adding this 1 ion each cell. I will follow the second approach. We need to represent carry-out values in the range 0 to 3. Thus, we need to signals to represent Carry out values.



(ii) Derive the truth table of your 1-bit module in (i).

$C1_{i-1}$	$C0_{i-1}$	X_i	$C1_i$	$C0_i$	Z_i
0	0	0	0	0	1
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	1	1

(iii) Derive minimized two-level sum-of-product equations for your 1-bit module circuit.

	00	01	11	10
0	1 0	0 1	1 3	0 2
1	1 4	0 5	1 7	0 6

$Z = (C0_{i-1} \oplus X_i)'$

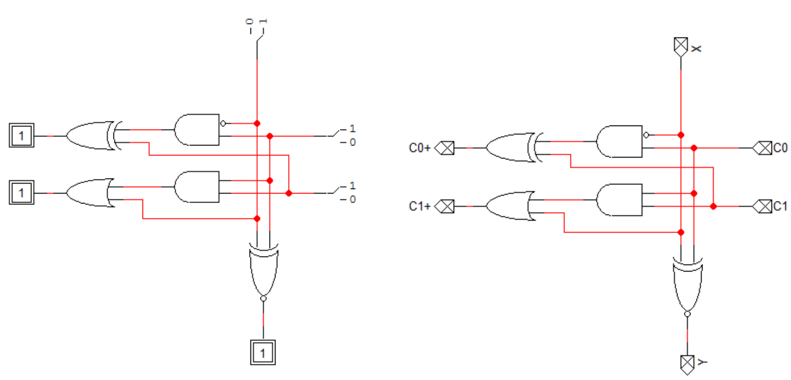
	00	01	11	10
0	0 0	0 1	0 3	1 2
1	1 4	1 5	1 7	0 6

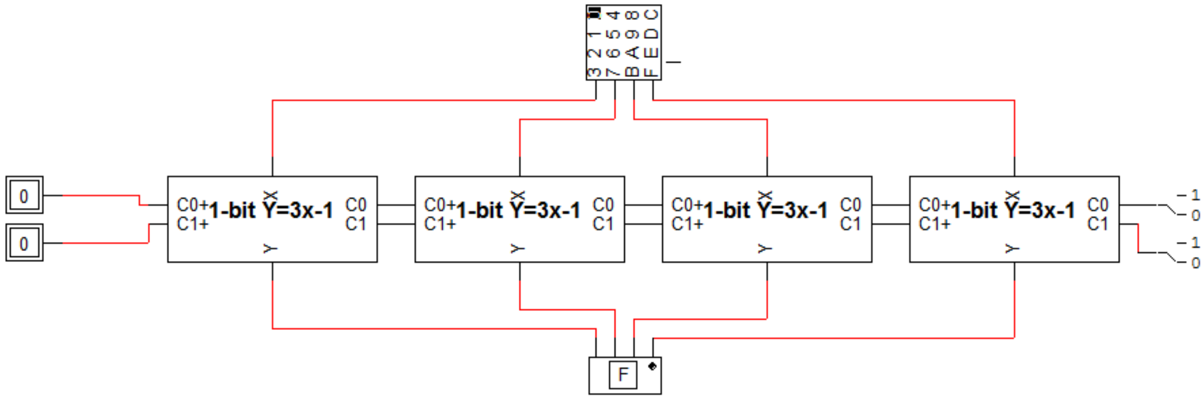
$C0_i = C1_{i-1}\ C0_{i-1}' + C1_{i-1}\ X_i + C1_{i-1}'\ C0_{i-1}\ X_i' = C1_{i-1}\ (C0_{i-1}' + X_i) + C1_{i-1}'\ C0_{i-1}\ X_i' = C1_{i-1} \oplus (C0_{i-1}\ X_i')$

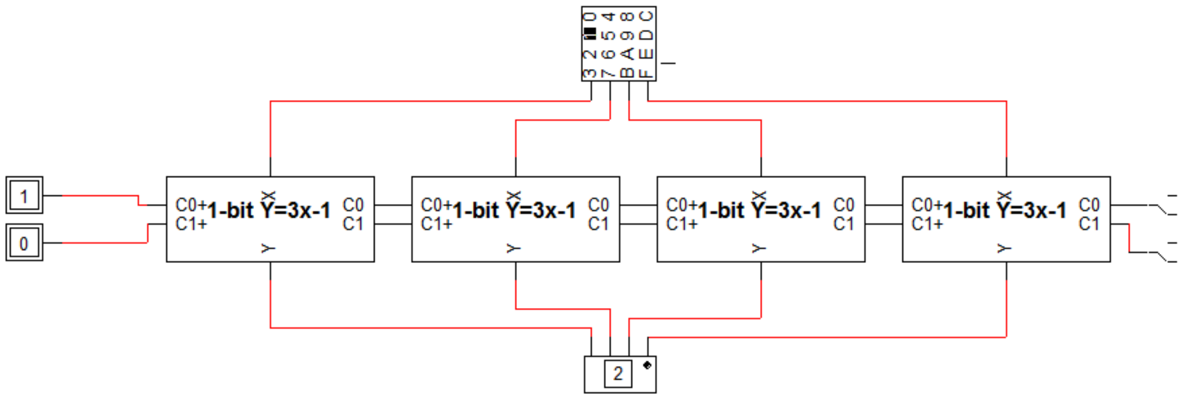
	00	01	11	10
0	0 0	1 1	1 3	0 2
1	0 4	1 5	1 7	1 6

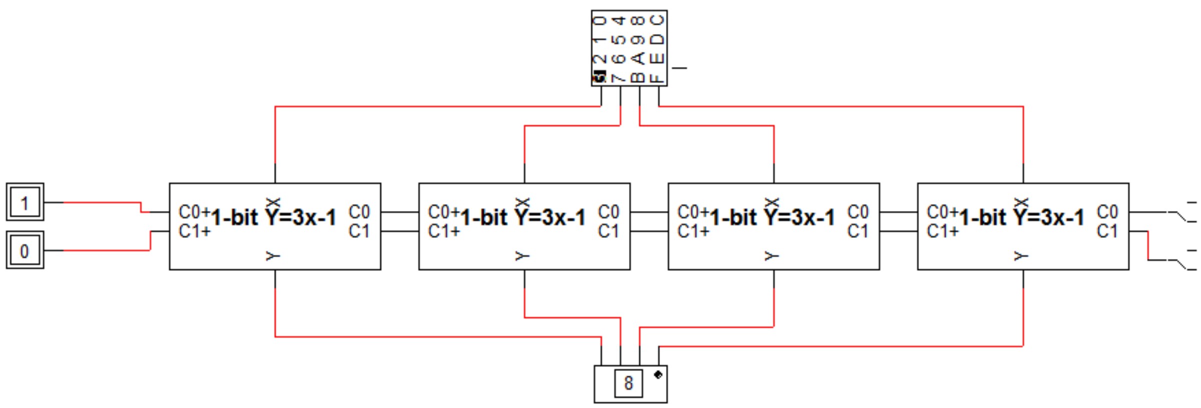
$C1_i = X_i + C1_{i-1}\ C0_{i-1}$

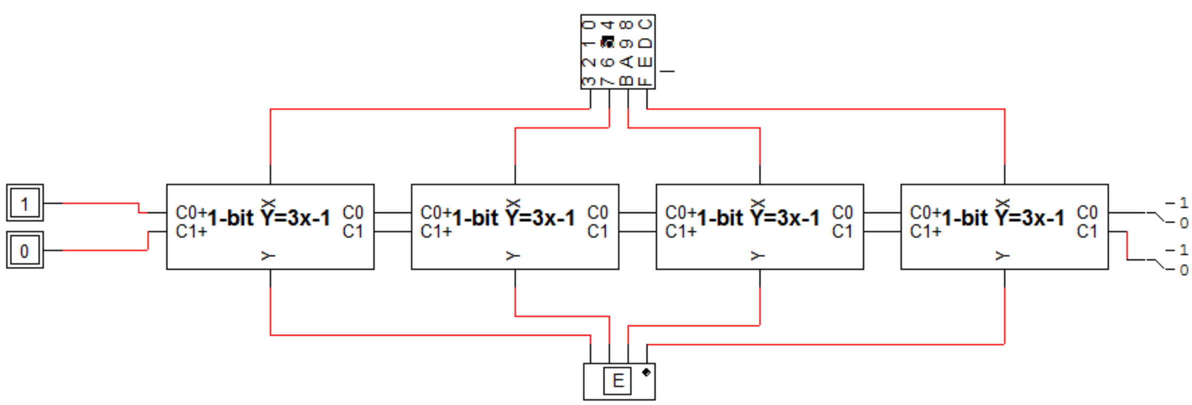
(iv) Verify the correctness of your design by modeling and simulating a circuit to compute the required equation assuming X is a 4-bit number using logicworks.

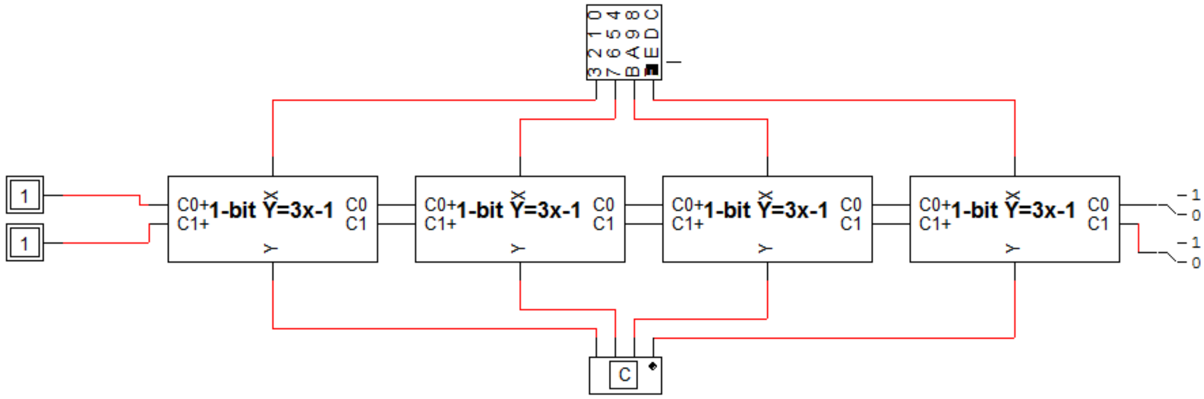


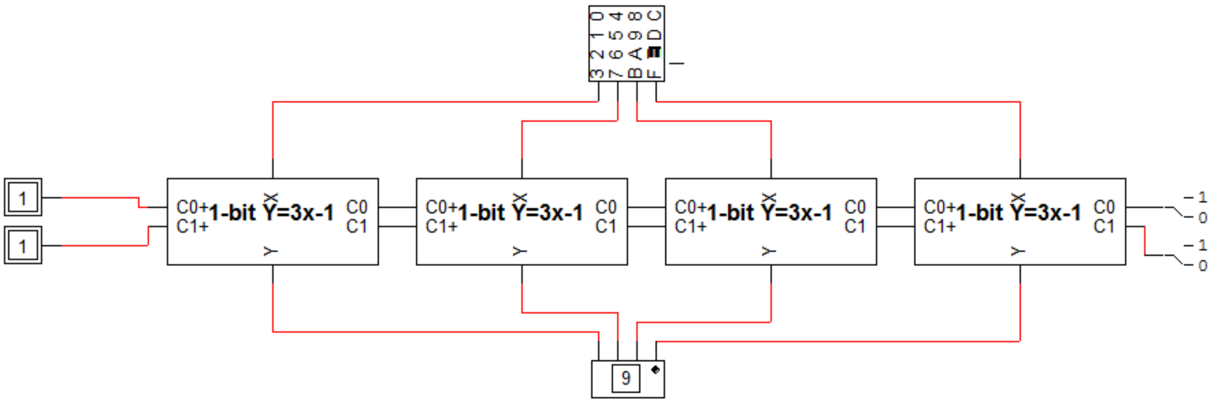

0
0
C0+1-bit Y=3x-1 C0
C1+ C1
F


1
0
C0+1-bit Y=3x-1 C0
C1+ C1
2


1
0
C0+1-bit Y=3x-1 C0
C1+ C1
8


1
0
C0+1-bit Y=3x-1 C0
C1+ C1
E





Note that for values whose correct result will not fit in 4-bits such as values ≥ 6 will not produce correct results. We need to use larger number of cells to ensure that the correct output will fit.