COE 405, Term 131

Design & Modeling of Digital Systems

HW# 1 Solution

Due date: Sunday, Sep. 29

Q.1. Consider the two functions f=a b c + a' b' c' and g=a b+a' c.

(i) Implement the function f using a single 4x1 MUX.

(ii) Compute the complement of f.

(iii) Compute the function f⊕g based on orthonormal basis expansion.

Q.2. It is required to design a combinational circuit that computes the equation Y=5*X, where X is an n-bit unsigned number.

(i) Design the circuit as a modular circuit where each module receives a single bit of the input, X_i.

(ii) Derive the truth table of your 1-bit module in (i).

(iii) Derive minimized two-level sum-of-product equations for your 1-bit module circuit.

(iv) Verify the correctness of your design by modeling and simulating a 4-bit circuit using logicworks.

(v) Assume that the delay of a gate is related to the number of its inputs, i.e. the delay of an inverter is 1, the delay of a 2-input gate is 2, etc. Compute the maximum propagation delay of your n-bit circuit.

(vi) Verify the correctness of your maximum propagation delay calculation by measuring the longest delay for a 4-bit circuit using logicworks.

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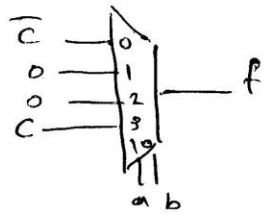
HW#1 Solution

Q1. $f = abc + \bar{a}\bar{b}\bar{c}$

$g = ab + \bar{a}c$

(i) $f = \bar{a}\bar{b}[\bar{c}] + \bar{a}b[0] + a\bar{b}[0] + ab[c]$



(ii) $\bar{f} = \bar{a}\bar{b}[c] + \bar{a}b[1] + a\bar{b}[1] + ab\bar{c}$

$= \bar{a}\bar{b}c + \bar{a}b + a\bar{b} + ab\bar{c}$

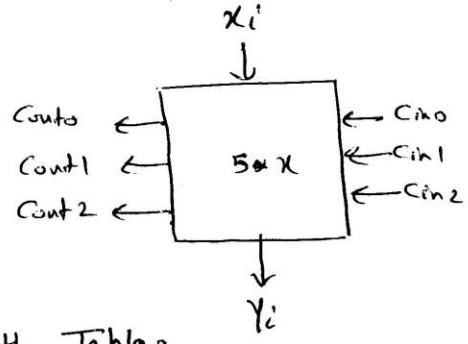
(iii) $g = \bar{a}\bar{b}[c] + \bar{a}b[c] + a\bar{b}[0] + ab[1]$

$f \oplus g = \bar{a}\bar{b}[1] + \bar{a}b[c] + a\bar{b}[0] + ab[\bar{c}]$

$= \bar{a}\bar{b} + \bar{a}bc + ab\bar{c}$

Q2. $Y = 5 * X$

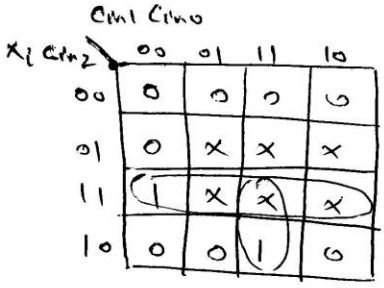
(i) By analyzing the problem, we can deduce that the largest carry-out is 4. Thus, we need 3 bits to be transferred between the modules. The interface for the 1-bit module is as follows:



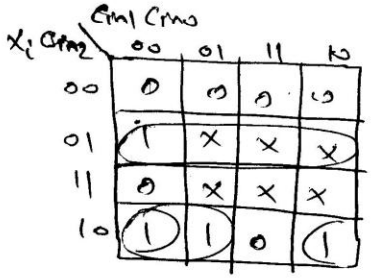
(ii) Truth Table:

x_i	Cin2	Cin1	Cin0	Cout2	Cout1	Cout0	Y_i
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	—	—	—	—
0	1	1	0	—	—	—	—
0	1	1	1	—	—	—	—
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	—	—	—	—
1	1	1	0	—	—	—	—
1	1	1	1	—	—	—	—

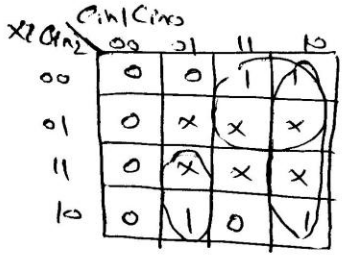
(iii)



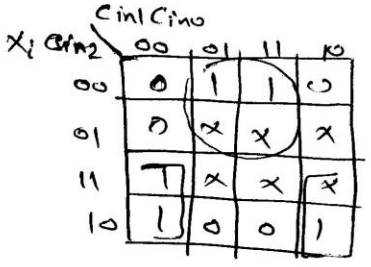
$$Cout_2 = x_i\, C_{in2} + x_i\, C_{in1}\, C_{in0}$$



$$Cout_1 = \bar{x}_i\, C_{in2} + x_i \bar{C}_{in2} \bar{C}_{in1} + x_i\, \bar{C}_{in2}\, \bar{C}_{in0}$$

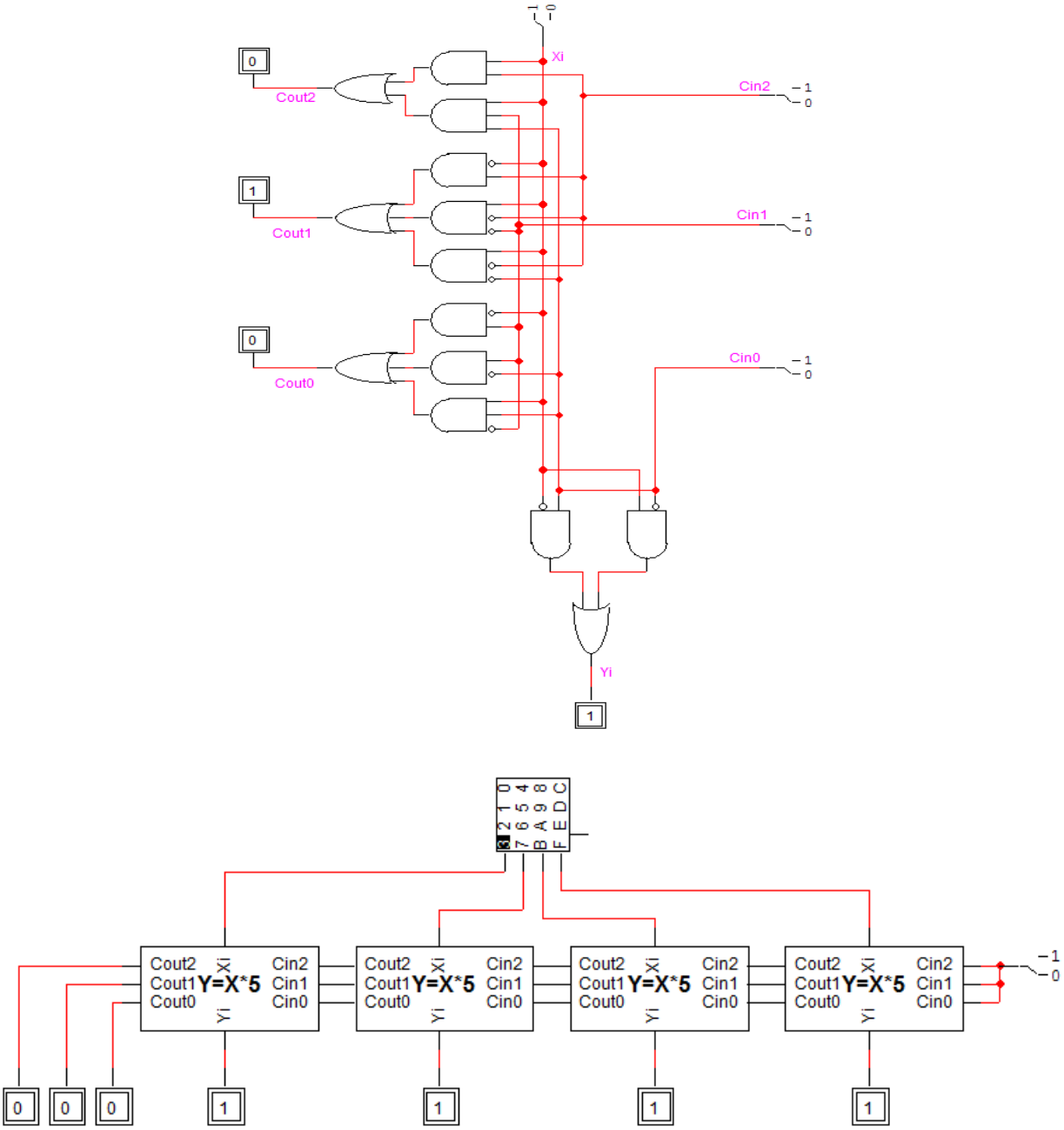


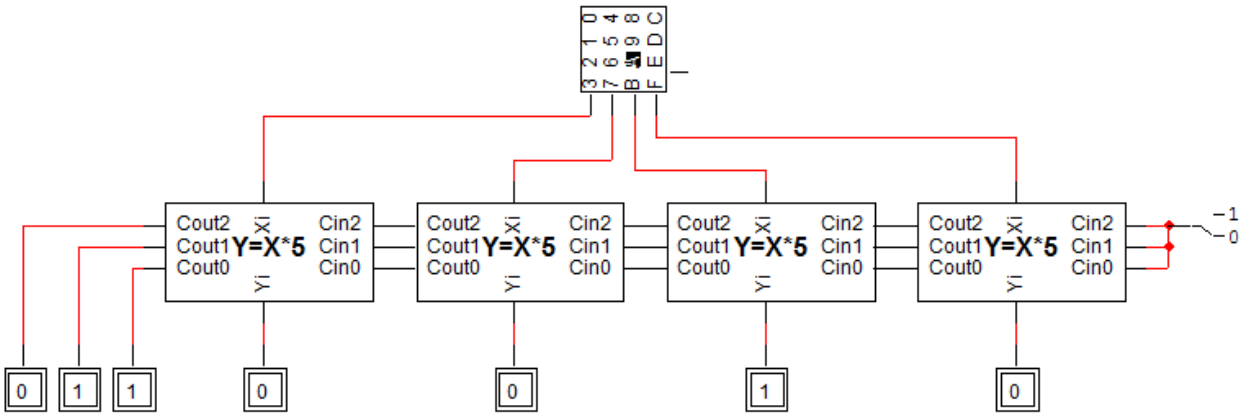
$$Cout_0 = \bar{x}_i\, C_{in1} + C_{in1}\, \bar{C}_{in0} + x_i\, \bar{C}_{in1}\, C_{in0}$$

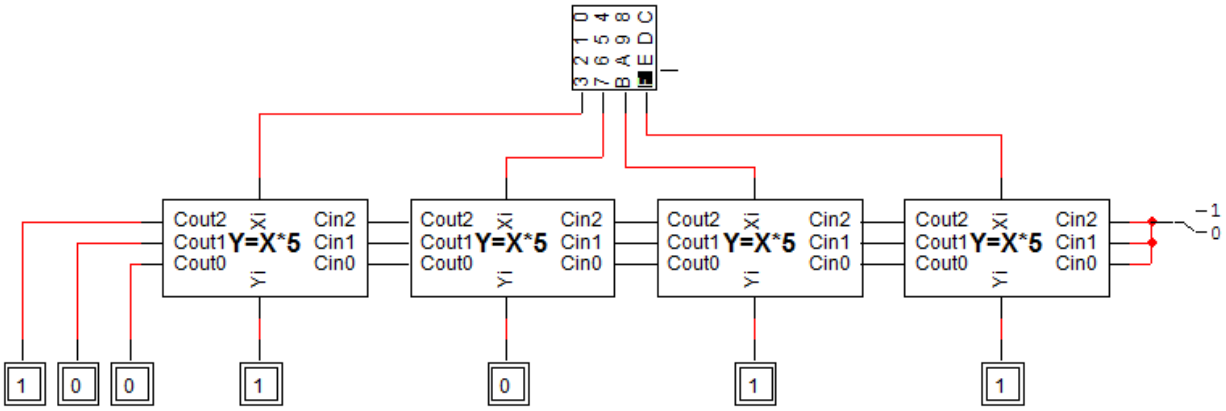


$$Y_i = \bar{x}_i\, C_{in0} + x_i\, \bar{C}_{in0}$$

(iv)







(v) To simplify the analysis, I add an inverter delay to any gate that has one of the inputs inverted. A very quick analysis by computing the longest delay across one cell, one can deduce that the longest delay across a cell is 7. Thus, having 4 cells the worst case delay is estimated to be 4*7=28.

(vi) To verify our analysis we changed X from 0 to 13 and computed the difference from the time X has changed (=2110) to the time when Y3 has changed (=2138) giving a total delay =2138-2110=28.