COE 405, Term 122

Design & Modeling of Digital Systems

HW# 1

Due date: Monday, Feb. 18

Q.1. Consider the two functions f=(a+bc)(a’+cd) and g=(a+b)(c+d).

- **(i)** Implement the function f using a single 4x1 MUX.
- **(ii)** Compute the complement of f.
- **(iii)** Compute the function $f \oplus g$ based on orthonormal basis expansion.

Q.2. You are required to design a circuit that computes the remainder of dividing a 4-bit number by 3. For example, if the input is 1010 the circuit produces a remainder output of 01 and if the input is 1111 the circuit produces an output of 00.

- **(i)** Derive the truth table of your circuit.
- **(ii)** Using k-map simplification, find the minimum sum-of-products expressions for each of the output signals.
- **(iii)** Perform multilevel optimizations if possible.
- **(iv)** Model your circuit using logic works and verify that it is working properly by simulation. Provide a snapshot of your simulation waveform.

Q.3. You are required to design a circuit that computes the remainder of dividing a N-bit number by 3, where N is a multiple of 4-bit numbers. The design needs to be modular in such a way that you design a cell that computes the remainder of dividing a 4-bit number by 3, and use this cell to construct the required circuit.

- **(i)** Derive the truth table of your basic cell.
- **(ii)** Using k-map simplification, find the minimum sum-of-products expressions for each of the output signals.
- **(iii)** Perform multilevel optimizations if possible.
- **(iv)** Model your cell using logic works and verify that it is working properly by simulation. Provide a snapshot of your simulation waveform.
- **(v)** Using your design cell, construct a circuit that computes the remainder of dividing an 8-bit number by 3. Verify the correct functionality of your circuit by simulation.