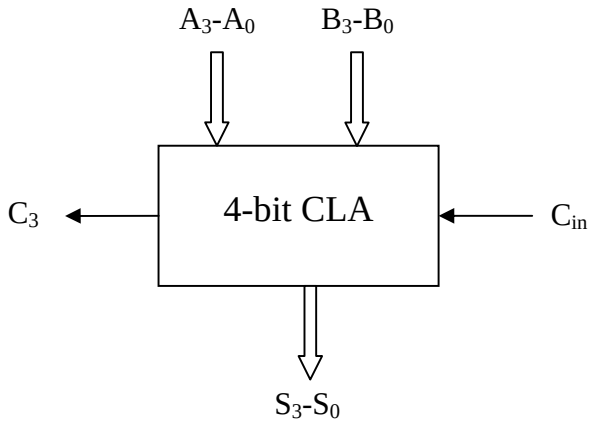
COE 405, Term 062

Design & Modeling of Digital Systems

HW# 1

Due date: Wednesday, March. 14

Q.1. Consider the 4-bit carry-look-ahead adder (CLA) block shown below:



(i) Describe an Entity **CLA4** in VHDL for this 4-bit CLA using exactly the same port names shown above.

(ii) Write in VHDL an Architecture **Conc** for this 4-bit CLA using concurrent statements.

(iii) Simulate the VHDL model **Conc** and verify that it is working properly. Include a snapshot of the simulated waveform.

(iv) Model an 8-bit adder, **Adder8**, based on cascading two CLA4 components by connecting the carryout of the first component to the carry-in of the second component.

(v) Simulate the VHDL model for the 8-bit adder and verify that it is working properly. Include a snapshot of the simulated waveform.

Q.2. It is required to model a 4-bit up-down counter with a synchronous rising-edge clock, and asynchronous reset. Assume that the counter has an input DIR when set to 0, it counts up otherwise it counts down.

(i) Describe an Entity **UDC4** in VHDL for the 4-bit up-down counter.

(ii) Model Architecture **Behavior** for the 4-bit up-down counter using a process.

(iii) Simulate the VHDL model **Behavior** and verify that it is working properly. Include a snapshot of the simulated waveform.

Q.3. It is required to design a sequential circuit that receives a serial input X, and produces a serial output Z, equivalent to 3*X, i.e., Z=3*X. The input coming to the X input is transmitted from the least significant bit to the most significant bit. The number of bits transmitted will be equal to the number of bits needed in the output Z. For example, for sending the decimal value 3, the input sequence 0011 will be transmitted and the output sequence 1001 will be produced.

(i) Show the state diagram of this circuit assuming **Mealy** model.

(ii) Model an Entity **Times3** and an Architecture **Behavior** for this circuit using a process. Assume that the circuit will have a synchronous reset and is rising-edge triggered.

(iii) Simulate the VHDL model **Behavior** and verify that it is working properly. Verify the correctness of your circuit by the following decimal numbers: 9, 10, and 15. Include a snapshot of the simulated waveform.