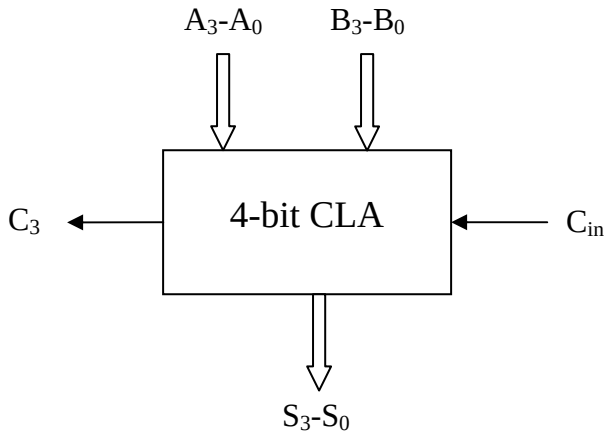
COE 405, Term 031

Design & Modeling of Digital Systems

HW# 1

Due date: Sunday, Oct. 12

Q.1. Consider the 4-bit carry-look-ahead adder (CLA) block shown below:



(i) Describe an Entity **CLA4** in VHDL for this 4-bit CLA using exactly the same port names shown above.

(ii) Write in VHDL an Architecture **Arch1** for this 4-bit CLA using concurrent statements.

(iii) Simulate the VHDL model **Arch1** and verify that it is working properly. Include a snapshot of the simulated waveform.

(iv) Write in VHDL an Architecture **Arch2** for this 4-bit CLA using gate-level description. Assume that the delay of an n-input gate is n ns.

(v) Simulate the VHDL model **Arch2** and verify that it is working properly. Determine by simulation the critical path of the adder. Include a snapshot of the simulated waveform.

Q.2. It is required to model a 4-bit register with a synchronous rising-edge clock, and asynchronous reset.

(i) Describe an Entity **FAR** in VHDL for a d-ff with a synchronous rising-edge clock, and asynchronous reset.

(ii) Model Architecture **Arch1** for the d-ff using a process.

(iii) Simulate the VHDL model **Arch1** of FAR and verify that it is working properly. Include a snapshot of the simulated waveform.

(iv) Describe an Entity **Reg4** in VHDL for the 4-bit register with asynchronous reset.

(v) Model Architecture **Arch1** for Reg4 using 4 instantiations of d-ff FAR.

(vi) Simulate the VHDL model **Arch1** of Reg4 and verify that it is working properly. Include a snapshot of the simulated waveform.

Q.3. It is required to model a 4-bit accumulator circuit using VHDL. The accumulator circuit shown below is designed using a 4-bit register with a synchronous rising-edge clock, CLK, and asynchronous reset, RST. When RST=0, the accumulator is reset to 0 asynchronously.

(i) Describe an Entity **ACC** in VHDL for the 4-bit accumulator.

(ii) Model Architecture **Arch1** for ACC using the 4-bit adder modeled in Q1 and the 4-bit register modeled in Q2.

(iii) Simulate the VHDL model **Arch1** of ACC and verify that it is working properly. Demonstrate that the accumulator can work as an up counter and also as a down counter by specifying proper input values. Include a snapshot of the simulated waveform.