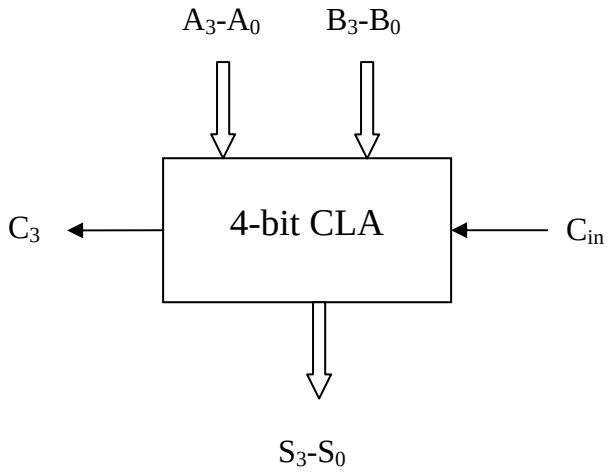
COE 405, Term 021

Design & Modeling of Digital Systems

HW# 1

<u>Due Date</u>: Sat. Oct. 5

Q.1. Consider the 4-bit carry-look-ahead adder (CLA) block shown below:



(i) Describe an Entity **CLA4** in VHDL for this 4-bit CLA using exactly the same port names shown above.

(ii) Write in VHDL an Architecture **Arch1** for this 4-bit CLA using concurrent statements.

(iii) Simulate the VHDL model **Arch1** and verify that it is working properly. Include a snapshot of the simulated waveform.

Q.2. Using the 4-bit CLA Entity modeled in Q1 do the following:

(i) Describe an Entity **Adder8** in VHDL for an 8-bit adder.

(ii) Model Architecture **Struct** for the 8-bit adder using two instantiations of the Entity **CLA4**.

(iii) Simulate the VHDL model **Struct** and verify that it is working properly. Include a snapshot of the simulated waveform.