COE 405

VHDL Synthesis Procedure Using Xilinx Tools

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Abstract

This tutorial will help you go throw the synthesis step of your VHDL modeling.

GENERAL STEPS

1- Install The Following Software:
   i. Xilinx Student Edition v4.2i (Software)
   ii. XSTools 4.0.2 (Software)

2- Using The Xilinx we will convert the VHDL to a bit file which can be downloaded into the FPGA later.

3- Using the XSTools we will download the bit file into the FPGA board.

GETTING STARTED

Installing the Xilinx Tools

1- Use the CD given to you to install the Xilinx tools from the folder "*Xilinx4.2*"

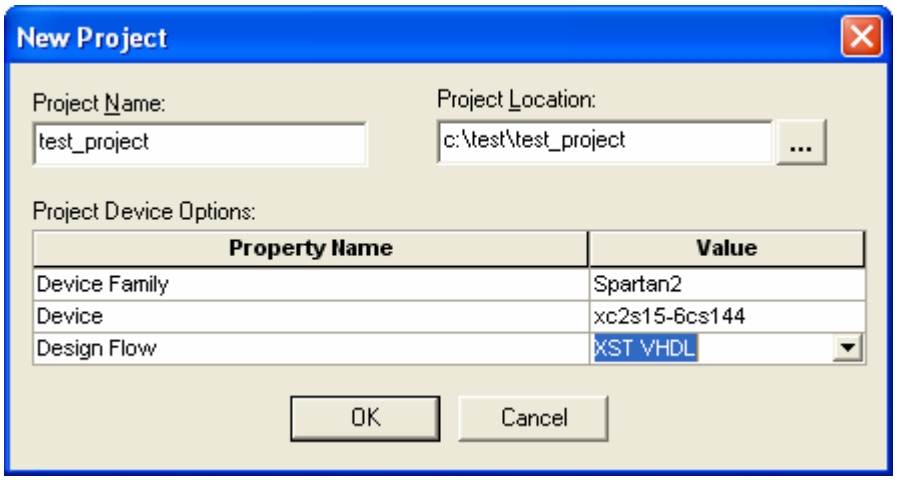
2- Choose the "Typical" setup and when asked for the serial number use this number"9990-6970-9169" and proceed in the installation.

3- You will be asked for the documentation CD, click cancel and continue.

4- Then Install the "XSTools 4.0.2" from the "*XSA-100 Board*" folder.

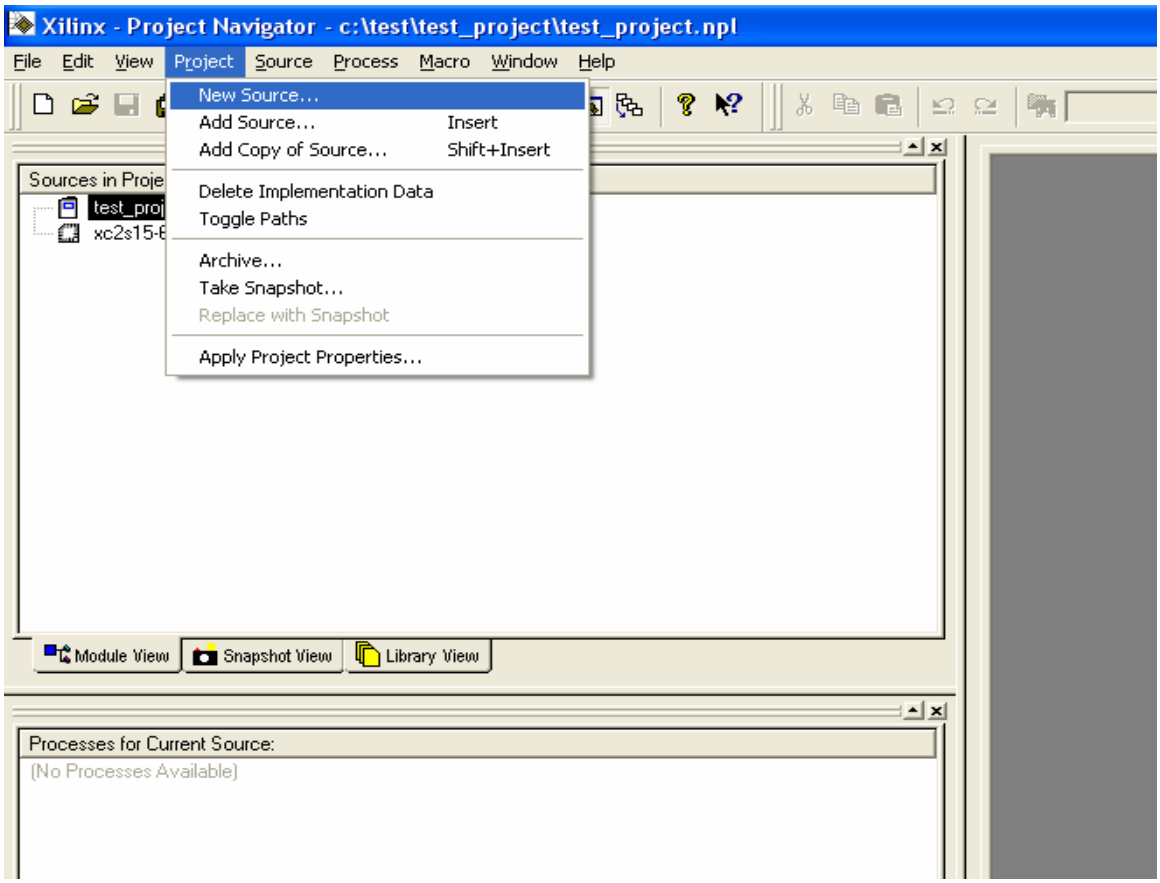
Converting your VHDL project into a BIT file

1- Run the "Project Navigator" from Program Menu → Xilinx ISE 4 → Project Navigator
2- From the File Menu click on "New Project" and you will see the following window

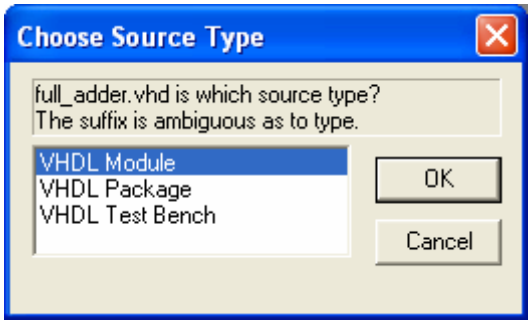


3- Fill in the project name and the project location and the device family and the device and the design flow, which we are using now (VHDL). And click Ok.

4- Go to the project menu and then click on “New Source” to write a new project or “Add Source” to add a ready VHDL file.



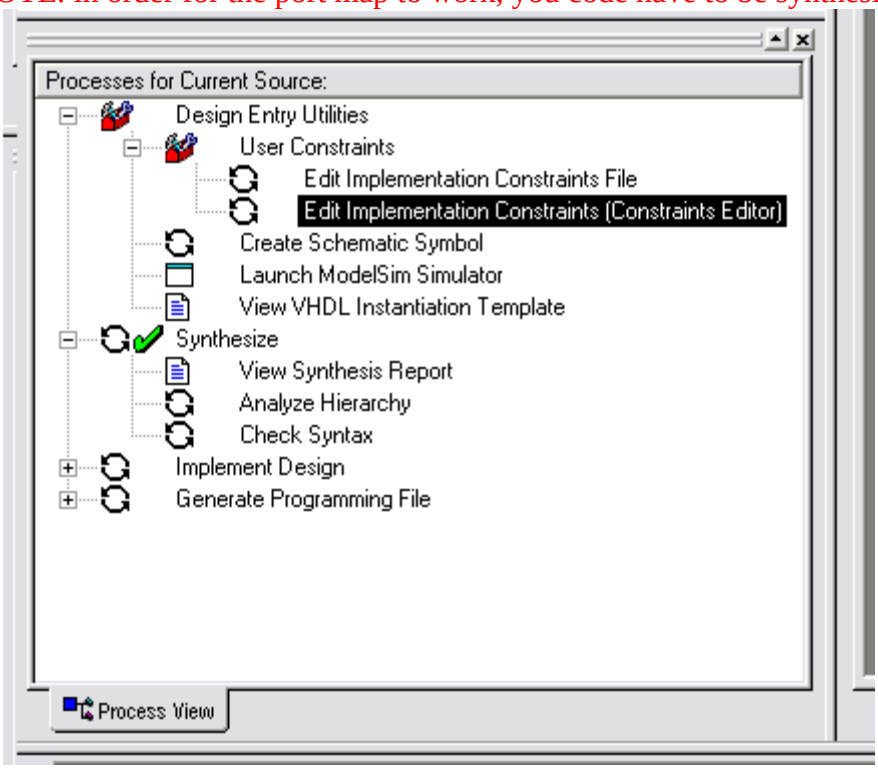
5- In our example here we will add a source file which models a full adder. And after the addition we will see the following screen.



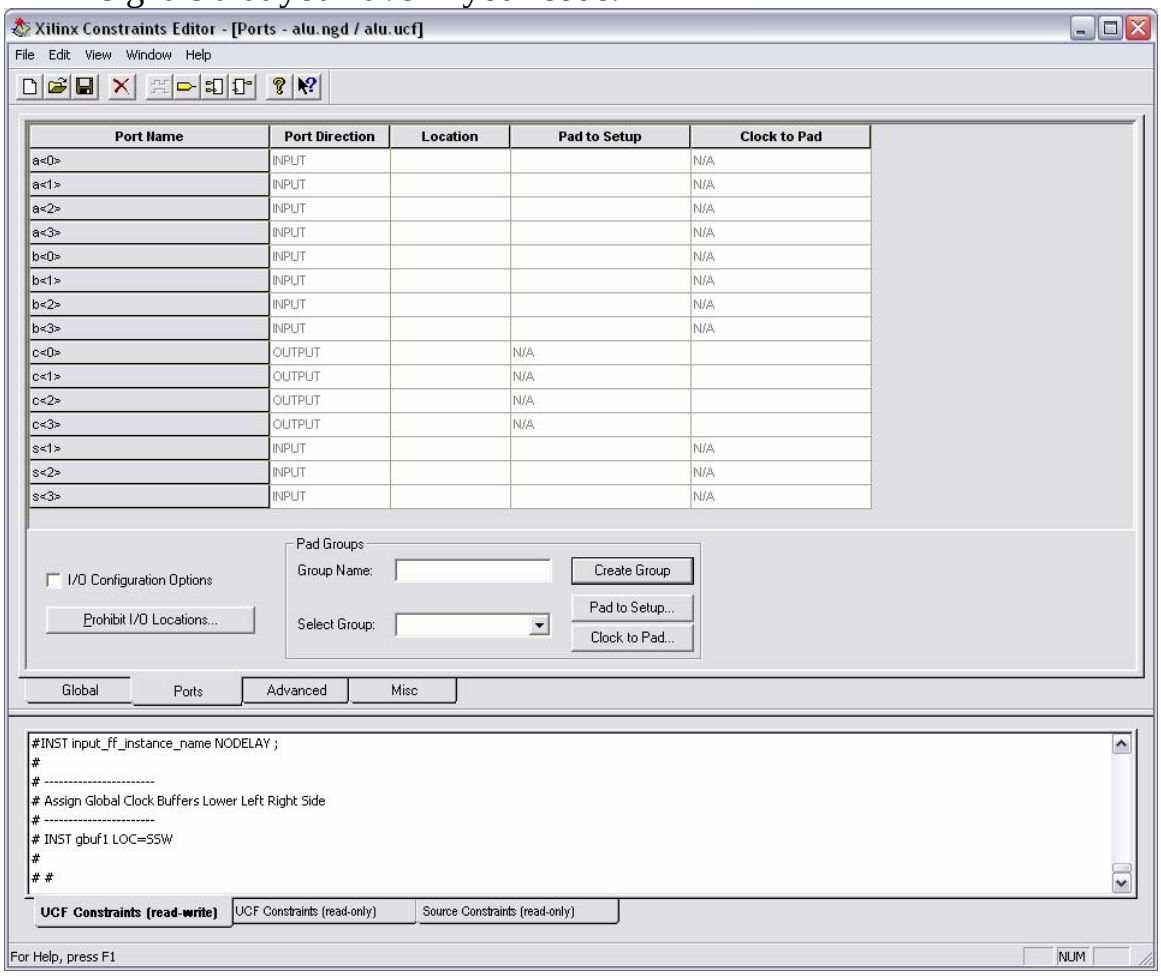
And we will choose the "VHDL Module" because our design is a module.

6- At this stage we should assign the ports that we want to map in the FPGA implementation. And that is used by the "Design Entry Utilities". NOW, go to the Process View → User Constraints → Edit Implementation Constraints (Constraints Editor). And double click it.

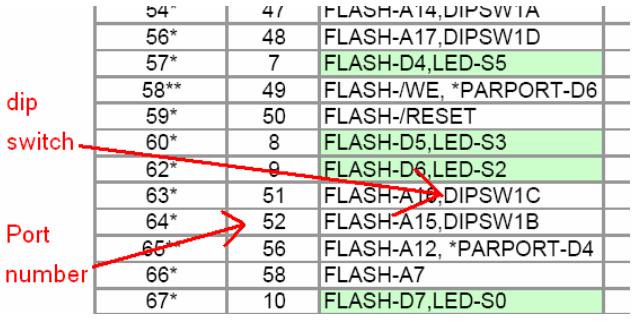
[NOTE: in order for the port map to work, you code have to be synthesizable]



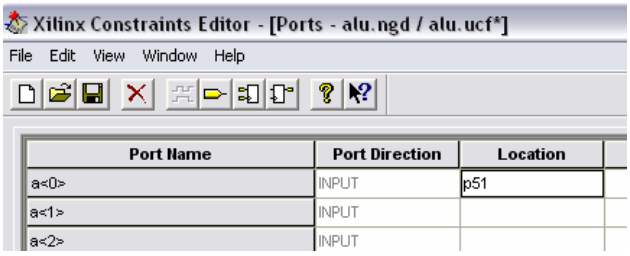
7- You will see now the following window, select the tap PORTS, and you can see that on the left side we have the variable and the signals that you have in your code.



8- Now, when assigning the ports we will have to see the FPGA manual because we need to know the ports for the 7 segment display or the dip switches, or even the pins. And that is achived by the PDF file that was included in the CD “xsa-manual-v1_2.pdf” so to page 31 and ou will see the pin connection of the XSA100.

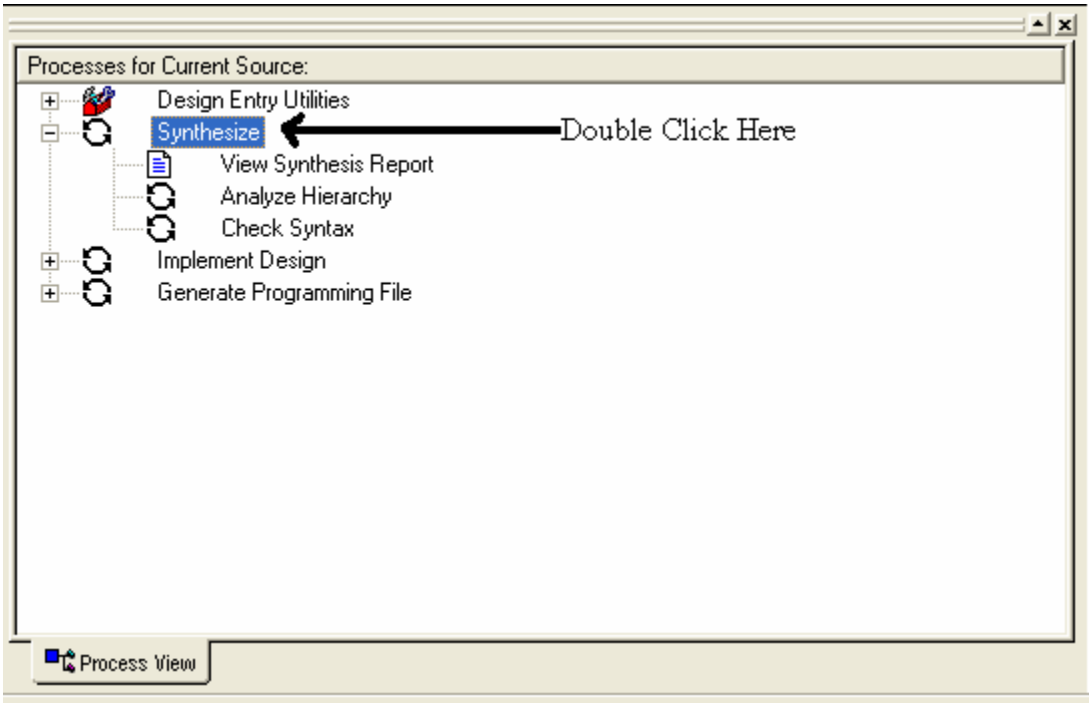


9- After that we can assign the ports to the input or the output we need. And we have to add the character P in front of the port number when we add it. (e.g. P51)



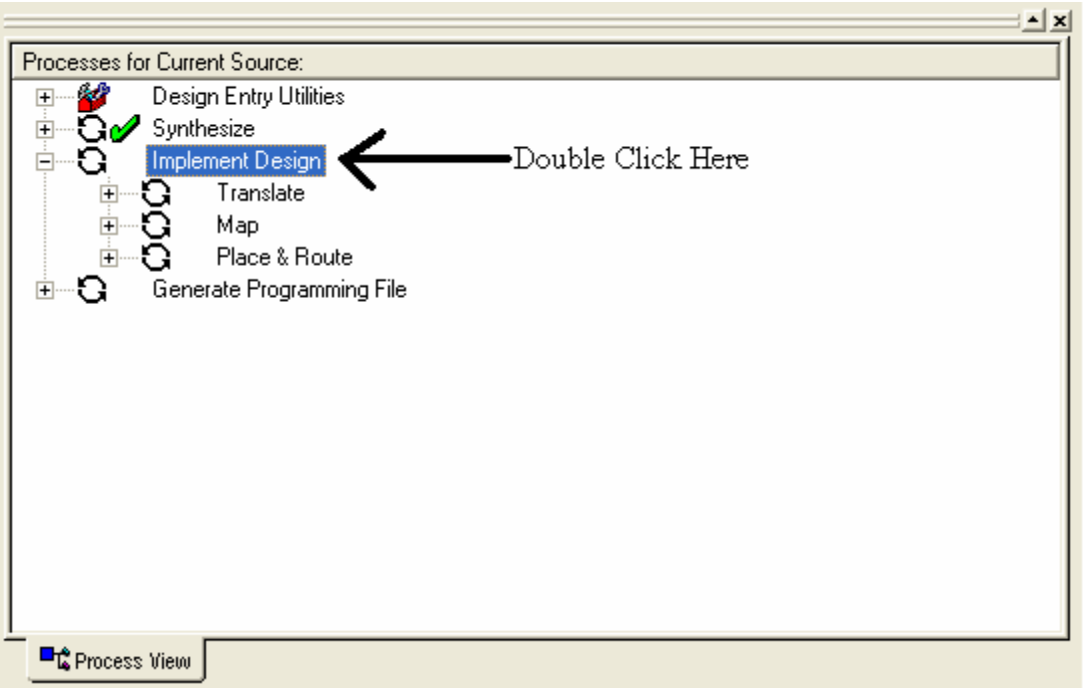
10- After you are done with all the assignment exit and save.

11- Now we have the code ready and we want to do the synthesis on it, so we will double click on “Synthesize” in the Process view as we see below.



12- If your code has no errors a check mark will show, but if there are some error with the code a cross will show. And when you see a cross you can check the errors by clicking on “View Synthesis Report” and you will find the errors at the end of the file and at which line they occurred.

13- After we are done with synthesis we will implement the design. And that is done by clicking on “Implement Design” in the Process View as we see below.

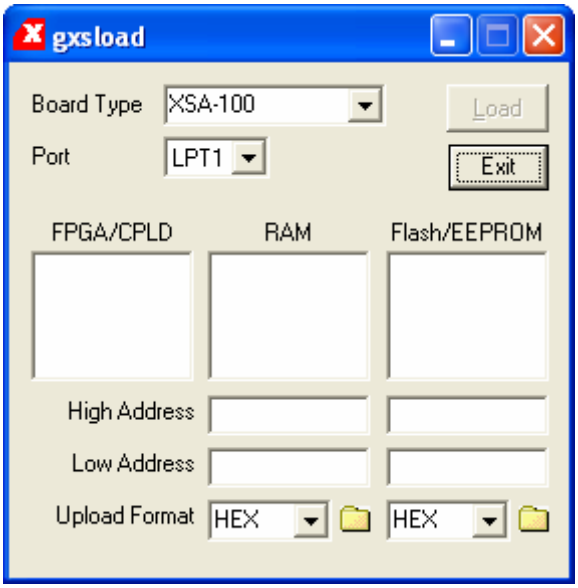


14- Now we have made the implementation we will do the last step in our first part which is to make the bit file and that is done by clicking on “Generate Programming File” which will produce the bit file in the Project Location (directory).

15- That will end our bit file generation and after that we will load the generated bit file in the FPGA board using the XSTools.

Loading the Bit File into the FPGA Board

1- Run the “GXSLOAD” program from Start→ Programs → XSTOOLS. And we will see the following screen.



2- Now, ***drag and drop*** your bit file into the "FPGA/CPLD" field.
3- Finally, JUST click on "load'.

Conclusions

Now your VHDL code is successfully loaded into the FPGA board.