

***KING FAHD UNIVERSITY OF PETROLEUM & MINERALS  
COLLEGE OF COMPUTER SCIENCES & ENGINEERING***

***COMPUTER ENGINEERING DEPARTMENT***

**COE 405 Design and Modeling of Digital Systems (3-0-3)  
Syllabus - Term 131**

**Catalog Description**

Review of sequential circuits design and analysis, Data path and control unit design, Design with Hardware Description languages (HDL), Design with Field-Programmable Gate Arrays (FPGAs), Block interfacing.

*Prerequisite:* COE 202 Logic Design

**Instructor** Dr. Aiman H. El-Maleh. Room: 22/407-5 Phone: 2811  
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**Office Hours**

**Course Objectives**

Introduce students to the design methodologies of digital systems with special emphasis on FPGA implementations.

**Course Learning Outcomes**

1. Data Path and Control Unit design
2. Digital systems modeling using hardware description languages (Verilog HDL)
3. Simulation of digital systems
4. Synthesis and FPGA implementation of digital systems

**Text book:** M. D. Ciletti, “Advanced Digital Design with the Verilog HDL,” (Prentice Hall), 2/e 2010.

**References:**

1. “Verilog Styles for Synthesis of Digital Systems”, David R. Smith and Paul D. Franzon, Prentice Hall, ISBN 0-201-61860-5
2. On line Verilog resources:
  - i. [http://www.doulos.com/knowhow/verilog\\_designers\\_guide/](http://www.doulos.com/knowhow/verilog_designers_guide/)
  - ii. [http://www.sutherland-hdl.com/online\\_verilog\\_ref\\_guide/vlog\\_ref\\_top.html](http://www.sutherland-hdl.com/online_verilog_ref_guide/vlog_ref_top.html)

## Grading Policy

Discussions	5%
Assignments	15%
Quizzes	10%
Midterm	20% (Sat. Nov. 9, 1:30 PM)
Project	25%
Final	25%

- Attendance will be taken regularly.
- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.
- Late assignments will be accepted (upto 3 days) but you will be penalized 10% per each late day.
- A student caught cheating in any of the assignments will get 0 out of 15%.
- No makeup will be made for missing Quizzes or Exams.

## Course Outline:

Week	Topics
1-2	Introduction to Digital Design Methodology. Review of combinational logic design. Review of Sequential circuit design, Mealy versus Moore Machines, timing constraints, State minimization, State assignment.
3-4	Design of a digital system by partitioning it into a Data Path and Control unit -- Design of DP and CU. Algorithmic State Machine (ASM) charts.
5-6	Introduction to logic design with Verilog: structural models of combinational logic, logic system, design verification and test methodology, propagation delay, truth table models of combinational and sequential logic with Verilog.
7-8	Logic design with behavioral models of combinational and sequential logic: continuous assignment models, dataflow/RTL models, algorithmic based models.
9-11	Synthesis of combinational and sequential logic: Introduction to synthesis, synthesis of combinational logic, synthesis of sequential logic, synthesis of three-state devices and bus interfaces, synthesis of explicit state machines, synthesis of implicit state machines, synthesis of loops.
12-13	Design and synthesis of Datapath controllers. Block interfacing.
14-15	Field Programmable Gate Arrays (FPGAs), FPGA technologies, Verilog based design flows for FPGAs, design and synthesis with FPGAs.