KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 405 Design and Modeling of Digital Systems
Syllabus - Term 062

Catalog Description

Design methodology. Hardware modeling basics. Modeling concurrency and timing aspects. Behavioral, structural, and data flow level modeling using hardware description languages (HDLs). System level modeling and design of practical processors, controllers, arithmetic units, etc. Translation of instruction sets to hardware models for software emulation. Case studies.

Prerequisite: COE 308 or consent of instructor

Instructor Dr. Aiman H. El-Maleh. Room: 22/318 Phone: 2811
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Office Hours SMW 10:00-10:50, and by appointment

Course Objectives

After successfully completing the course, students will be able to:

1. Master the hardware description language, VHDL, for the design (specification, modeling, simulation, and synthesis) of digital systems using programmable logic or VLSI components.

2. Design complete digital systems starting from the concept, advancing through the modeling, simulation, synthesis, and test, by using different styles in VHDL, namely structural, dataflow, and behavioral, for describing the architecture.

Course Learning Outcomes

1. Ability to design a digital system based on VHDL including modeling, simulation, and synthesis.

2. Ability to use CAD tools for the analysis and verification of digital designs.

3. Ability to demonstrate self-learning capability.

4. Ability to work in a team.

Text Book : Zainalabedin Navabi, "VHDL: Analysis and Modeling of Digital Systems", McGraw-Hill, Inc., 2nd edition, 1998.

Grading Policy

Assignments	15%	
Quizzes	10%	
Exam I	15%	**(Th., March 29, 1:00 PM)**
Exam II	20%	**(Th. , May 10, 1:00 PM)**
Project	20%	
Final	20%	

- Attendance will be taken regularly.
- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.
- Late assignments will be accepted (upto 3 days) but you will be penalized 10% per each late day.
- A student caught cheating in any of the assignments will get 0 out of 15%.
- No makeup will be made for missing Quizzes or Exams.

Course Outline:

	Topic	**Content**	**Reference**
1.	Structured Design Methodologies	Digital System Design, Abstraction hierarchy, Types of Behavioral Descriptions, Digital Design Space & Design Decomposition.	Ch. 1
2.	VHDL Quick Overview	Design Partitioning & Top-Down Design, Design Entities, Signals vs. Variables, Architectural Bodies, Different Design Views, Behavioral Model, Dataflow Model, Structural Model.	Ch. 3
3.	VHDL Language Basics	Lexical Elements, Data Types (Scalars & Composites), Type Conversion, Attributes, Classes of objects, Operators & Precedence, Overloading.	Ch. 7
4.	Signals, Delays & Concurrency	Variables vs. Signals, Sequential vs. Concurrent Constructs, Signal Propagation Delay & Delay types, Transactions, Events and Transaction Scheduling, Signal Attributes.	Ch. 4
5.	Design & Modeling Tools	Tutorials on available Simulators and Design Tools.	Handout
6.	Structural Models	Structural Models, Configuration Statement, Modeling Iterative/Regular Structures, Test Benches.	Ch. 5
7.	Design Organization & Parameterization	Packages & Libraries, Design Parameterization, Design Configuration & General Purpose Test Bench.	Ch. 6
8.	Dataflow Models	Concurrent Signal Assignment, Block	Ch. 8

		Statements, Guards, Resolution Functions, Resolved Signals and Signal Kinds, Data Flow Moore & Mealy Models, Data & Control Path Data Flow Models.	
9.	Behavioral Models	Process & Wait Statements, Assert Statement, General Algorithmic Model, Moore and Mealy Machine Algorithmic Models, Data & Control Path Design.	Ch. 9
10.	Writing Test Benches	Types of Test Benches, Examples	Handout
11.	Introduction to VHDL Synthesis	Combinational, Sequential Logic Synthesis, State Machine Synthesis, VHDL Coding Styles for Synthesis.	Handout, App. C
12.	CPU Design Example	Behavioral Modeling of CPU, Datapath and Control Unit Modeling, CPU-Memory Interface.	Ch.10, 11.