College of Computer Science & Engineering

Computer Engineering Department

Design and Modeling of Digital Systems
COE 405 (3-0-3)

Course Syllabus **(031)**

Instructor

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Office Hours SMW 11:00-12:00; UT 2:30-3:30 (and by appointment)

Course Objectives:

Mastering the hardware description language, VHDL, for the design (specification, simulation, and synthesis) of digital systems. Designing complete digital systems starting from the concept, advancing through the simulation, synthesis, and test, by using different styles in VHDL, namely structural, dataflow, and behavioral, for describing the architecture.

Prerequisite: COE 308 or Consent of Instructor

Text Book : Zainalabedin Navabi, "VHDL: Analysis and Modeling of Digital Systems", McGraw-Hill, Inc., 2nd edition, 1998.

Grading Policy

Assignments	20%
Quizzes	10%
Project	25%
Midterm	20%
Final	25%

- Assignments are to be submitted in class in the specified due date.
- Late assignments will be accepted but will be penalized 10% per each late day.
- The project is to be performed by teams of two students.

Course Outline:

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	Topic		Reference
1.	Structured Design Methodologies	Digital System Design, Abstraction hierarchy, Types of Behavioral Descriptions The Digital Design Space & Design Decomposition.	Ch. 1
2.	VHDL Quick Overview	Design Partitioning & Top-Down Design. Design Entities, Signals vs. Variables, Architectural Bodies, Different design views, behavioral model, dataflow model, structural models.	Ch. 3
3.	VHDL Language Basics	Lexical Elements, Data Types (Scalars & Composites), Type Conversion, Attributes, Classes of objects. Operators & Precedence, Overloading.	Ch. 7
4.	Signals, Delays & Concurrency.	Variables vs. Signals, sequential vs concurrent constructs, Signal Propagation Delay & Delay types, Transactions, Events and Transaction Scheduling, Signal Attributes.	Ch. 4
5.	Design & Modeling Tools	Tutorials on available Simulators and Design Tools	Handout
6.	Structural Models	Structural Models, Configuration Statement, Modeling Iterative/Regular Structures, and Test Benches.	Ch. 5
7.	Design Organization & Parameterization	Packages & Libraries. Design Parameterization, Design Configuration & General purpose test bench.	Ch. 6
8.	Dataflow Models	Concurrent Signal Assignment, Block statements, Guards, Resolution functions, Resolved Signals and Signal Kinds, Data Flow Moore & Mealy Models, Data & Control Path Data Flow Models.	Ch. 8
9.	Behavioral Models	Process & Wait Statements, Assert Statement, General Algorithmic Model, Moore and Mealy Machine Algorithmic Models, Data & Control Path Design.	Ch. 9
10.	Writing Test Benches	Types of Test Benches, Examples	Handout
11.	Introduction to VHDL Synthesis	Combinational, sequential logic synthesis, state machine synthesis. VHDL coding styles for synthesis.	Handout
12.	CPU Design Example		Ch.10, 11.