March 25, 2017

COMPUTER ENGINEERING DEPARTMENT

COE 405

DESIGN & MODELING OF DIGITAL SYSTEMS

Midterm Exam

Second Semester (162)

Time: 1:00-3:00 PM

Student Name : _KEY_____

Student ID. : _____

Question	Max Points	Score
Q1	10	
Q2	10	
Q3	8	
Q4	8	
Q5	10	
Q6	14	
Total	60	

Dr. Aiman El-Maleh

[10 Points]

(Q1) Consider the function: $F(A,B,C,D) = (A \oplus B)(C \oplus D)$

(i) Compute the expansion of F using the **Orthonormal Basis** $\{\varnothing_1 = \overline{A}\,\overline{B}, \varnothing_2 = \overline{A}B, \varnothing_3 = A\overline{B}, \varnothing_4 = AB\}$.

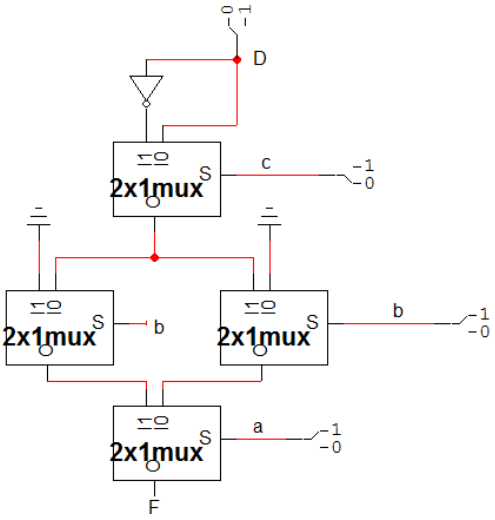
F = A'B' [0] + A'B [C⊕D] + AB' [C⊕D] + AB[0]

(ii) Compute the function $\overline{F}$ utilizing the orthonormal based expansion of the function.

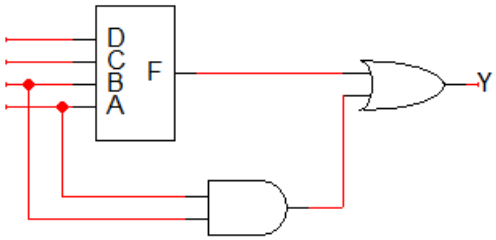
F' = A'B' [1] + A'B [C⊕D]' + AB' [C⊕D]' + AB[1]
= (A⊕B)' + (C⊕D)'(A⊕B)= (A⊕B)' + (C⊕D)'

(iii) Implement the function F using <u>minimal</u> number of 2x1 MUXs and inverters.

F = A' [B' [0] + B [C⊕D]] + A [B' [C⊕D] + B[0]]



(iv) Suppose that the function F is part of a circuit whose output is Y as shown below. Simplify the equation of F to minimum area.



We simply the function using A B as a don't care condition.

	00	01	11	10
00	0 0	0 1	0 3	0 2
01	0 4	1 5	0 7	1 6
11	?12	?13	?15	?14
10	0 8	1 9	011	110

F = B C' D + B C D' + A C' D + A C D' = (A+B)(C⊕D)

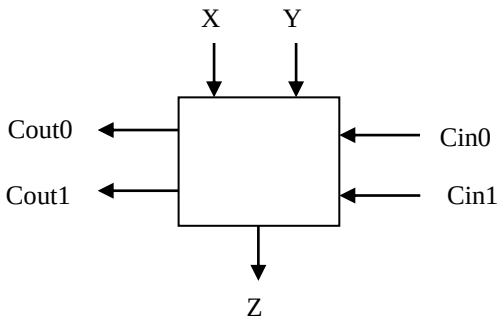
[10 Points]

(Q2) It is required to design an **<u>iterative</u>** combinational circuit that receives an **n-bit** signed 2's complement number X and computes the equation Z=3*X-Y. The design should be based on a one-bit cell (i.e., processing one bit of X_i and Y_i) that can be copied n times to construct the n-bit design.

(i) Determine the inputs and outputs for a one-bit cell. Clearly explain the meaning of signal values for the interface signals between the cells.

We need to pass between cells the following information, which is encoded using 2-bits as shown below:

Cin1	Cin0	Meaning
0	0	No carry or borrow
0	1	Carry=1
1	0	Carry=2
1	1	Borrow=1



(ii) Derive the truth table for a one-bit cell.

Cin1	Cin0	X	Y	Cout1	Cout0	Z
0	0	0	0	0	0	0
0	0	0	1	1	1	1
0	0	1	0	0	1	1
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	0	0	0
0	1	1	0	1	0	0
0	1	1	1	0	1	1
1	0	0	0	0	1	0
1	0	0	1	0	0	1
1	0	1	0	1	0	1
1	0	1	1	1	0	0
1	1	0	0	1	1	1
1	1	0	1	1	1	0
1	1	1	0	0	1	0
1	1	1	1	0	0	1

[8 Points]

(Q3) It is required to design a sequential circuit using Mealy model that computes the equation Z=3*X-Y, where X and Y are signed 2's complement numbers that will be fed serially. Assume that the circuit has an asynchronous Reset input that resets the machine to the reset state. Draw the state diagram or the state table for your sequential circuit.

We will need 4 states as shown below with S0 being the reset state.

State	Meaning
S0	No carry or borrow
S1	Carry=1
S2	Carry=2
S2	Borrow=1

The state table is giben below:

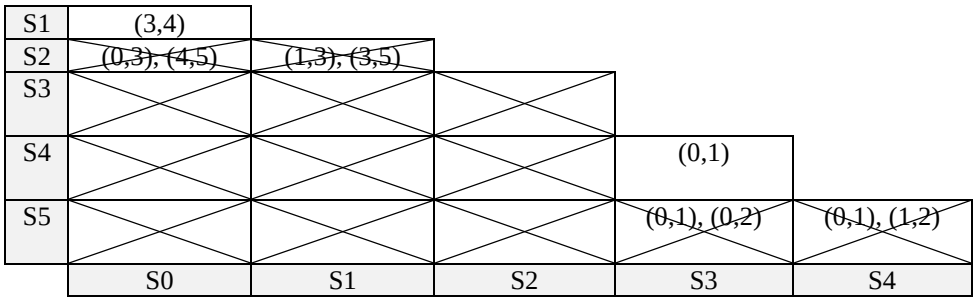
Current State	X	Y	Next State	Z
S0	0	0	S0	0
S0	0	1	S3	1
S0	1	0	S1	1
S0	1	1	S1	0
S1	0	0	S0	1
S1	0	1	S0	0
S1	1	0	S2	0
S1	1	1	S1	1
S2	0	0	S1	0
S2	0	1	S0	1
S2	1	0	S2	1
S2	1	1	S2	0
S3	0	0	S3	1
S3	0	1	S3	0
S3	1	0	S1	0
S3	1	1	S0	1

[8 Points]

(Q4) Consider the given Moore FSM that has 6 states, one input (X) and one output (Z), represented by the following state table:

Present State	Next State		Output
	X=0	X=1	Z
S0	S0	S4	0
S1	S1	S3	0
S2	S3	S5	0
S3	S0	S0	1
S4	S0	S1	1
S5	S1	S2	1

(i) Determine the equivalent states.



Equivalent states are: (S0, S1), (S2), (S3, S4) , (S5).

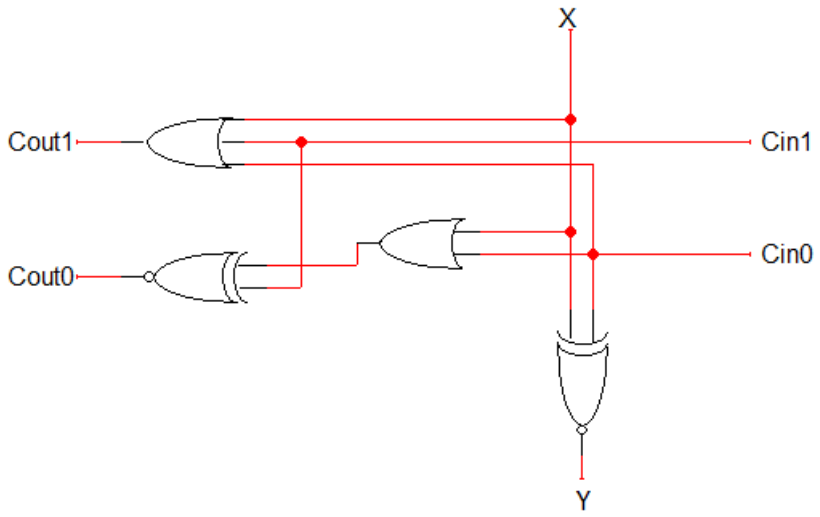
(ii) Reduce the state table into the minimum number of states and show the reduced state table.

The reduced state table is:

Present State	Next State		Output
	X=0	X=1	Z
S0	S0	S3	0
S2	S3	S5	0
S3	S0	S0	1
S5	S0	S2	1

[10 Points]

(Q5) Consider the combinational circuit given below modeling a 1-bit cell for computing the equation Y=X-3, which has three inputs X, Cin1 and Cin0 and three outputs Y, Cout1, and Cout0:



(i) Write a Verilog model to model the 1-bit cell design of the circuit using assign statements.

```
module OneCellXM3 (output Cout1, Cout0, Y, input Cin1, Cin0, X);

    assign Y = Cin0 ~^  X;

    assign Cout1 = Cin1 | Cin0 |  X;

    assign Cout0 = Cin1 ~^ (Cin0 |  X);

endmodule
```

(ii) Write a Verilog model for modeling a 3-bit circuit for computing the equation Y=X-3 by instantiating three copies of this cell and making necessary connections. Note that the carry in signals for the first cell should be all connected to 0.

```
module DXM3 (output Cout1, Cout0, output [2:0] Y, input [2:0] X);

wire [1:0] C1, C0;

OneCellXM3 M1 (C1[0], C0[0], Y[0], 0, 0, X[0]);
OneCellXM3 M2 (C1[1], C0[1], Y[1], C1[0], C0[0], X[1]);
OneCellXM3 M3 (Cout1, Cout0, Y[2], C1[1], C0[1], X[2]);

endmodule
```

(iii) Write a Verilog test bench that tests your 3-bit circuit by applying the following input patterns to your cell (X2X1X0)={011, 100, 111}.

```
module DXM3_Test();

reg [2:0] X;
wire Cout1, Cout0;
wire [2:0] Y;

DXM3 M1 (Cout1, Cout0, Y, X);

initial begin

X=3'b011;

#100 X=3'b100;

#100 X=3'b111;

end

endmodule
```

[14 Points]

(Q6) Consider the state table given below of the sequential circuit that computes the equation Y=X-3 using Mealy model, where X is a signed number in 2's complement that will be fed serially. Assume that the circuit has an asynchronous Reset input that resets the machine to the reset state.

Present State	**Next State, Y**	
	X=0	**X=1**
S0	S1, 1	S2, 0
S1	S2, 0	S2, 1
S2	S2, 1	S3, 0
S3	S3, 0	S3, 1

(i) Write a behavioral Verilog model for modeling your sequential circuit.

```
module YXM3 (output reg Y, input X, Reset, CLK);

        parameter S0 = 2'b00;
        parameter S1 = 2'b01;
        parameter S2 = 2'b10;
        parameter S3 = 2'b11;

reg [1:0] CS, NS;

always @ (posedge CLK, posedge Reset)
begin
  if (Reset)
     CS <= S0;
  else
    CS <= NS;
end

always @ (X or CS)
begin
Y = 0;
case (CS)
S0:  if (X)  NS=S2;   else begin Y=1; NS=S1; end
S1: if (X) begin Y=1; NS=S2; end  else NS=S2;
S2:  if (X) NS=S3;  else begin Y=1; NS=S2; end
S3:  if (X) begin Y=1; NS=S3; end else NS=S3;

endcase
end

endmodule
```

(ii) Write a Verilog test bench to test the correctness of your design for the following input values: {X=3} and {X=7}. You test bench should generate the clock internally using a clok period of 100 ps with 50% duty cycle. Reset the machine before applying each input sequence.

```
module YXM3_TB() ;

reg CLK, Reset, X ;
wire Y ;

YXM3 M1 (Y, X, Reset, CLK);

initial begin

CLK = 0 ; forever #50 CLK = ~ CLK ;

end

initial begin

//Applying X=3
@(negedge CLK) Reset=1;
@(negedge CLK) Reset=0; X=1;
@(negedge CLK) X=1;
@(negedge CLK) X=0;

//Applying X=7
@(negedge CLK) Reset=1;
@(negedge CLK) Reset=0; X=1;
@(negedge CLK) X=1;
@(negedge CLK) X=1;

end
endmodule
```