KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 405 Design and Modeling of Digital Systems

Term 162 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	U 5/2	Syllabus & Course Introduction. Introduction to Digital Design Methodology.	Chapter 1
2	T 7/2	Digital System Design Cycle, Architecture Design Example.	Chapter 1
3	TH 9/2	Design Space and Evaluation Space, Digital System Complexity. Dealing with Design Complexity, Design Hierarchy, Abstractions, Design Domains & Levels of Abstraction, Design Methods. Design vs. Synthesis, Synthesis Process, Circuit Synthesis.	Chapter 1
4	U 12/2	Hardware Description Languages, Design Automation & CAD Tools. Definitions: implicant, Prime Implicant, Essential Prime Implicant. Minimum cover, Minimal cover or irredundant cover. Sum of Product (SOP) Simplification Procedure. Shannon's Expansion, Boolean Expansion Based on Orthonormal Basis. Don't Care Conditions.	Chapter 1 & 2
5	T 14/2	SOP Simplification Procedure using Don't Cares, Product of Sum (POS) Simplification. Combinational Circuits Design Procedure, Iterative Design.	Chapter 2
	T 14/2 (Makeup)	Iterative Design. Decoders, Implementing Functions using Decoders. Multiplexers, Implementing Functions using Multiplexers.	Chapter 2
6	TH 16/2	Introduction to Verilog, Why use HDL?, Definition of a Module. Gate-level modeling, Verilog primitives. Verilog Syntax, Verilog Data Types. Module instantiation.	4.1-4.2
7	U 19/2	No Class.	
8	T 21/2	Organization of a Testbench for Verifying a Unit Under Test (UUT), Testbench Template, Propagation Delay, Inertial Delay, Assign Statement, Propagation Delay & Continuous Assignment. Sequential Circuit Models: Mealy vs Moore. Sequential Circuit Design.	4.2-4.4 & Chapter 3
9	TH 23/2	Sequential Circuit Design Examples.	Chapter 3

10	U 26/2	State Minimization.	Chapter 3
11	T 28/2	Sequential Circuit Timing, Timing Constraints, FF set up time, Clock to Q delay, FF hold time, Clock Skew. **(Quiz#1)**	Chapter 3
12	TH 2/3	Peak to Peak Jitter, Hold Time violation, metastability, synchronizing flip-flops. Behavioral Modeling, Data Types for Behavioral Modeling, Assign Statement, Verilog Operators, Always Block, Procedural Assignment.	Chapter 3 & 5.1-5.3
13	U 5/3	Wire vs. Reg, Algorithm-Based Models, if statement, Case statement. Behavioral Models of Multiplexor, Encoder, Decoder. D Latch, D Flip-flop (synchronous & asynchronous reset).	5.6-5.9
14	T 7/3	D Flip-flop (synchronous & asynchronous reset), Data Flow/ RTL Models: Shifter. Behavioral Models of Multiplexor. Encoder, Decoder. Seven Segment Display Decoder, FSM Modeling, FSM Test Bench, Parallel Load Register.	5.6-5.11, 5.14
15	TH 9/3	Shift Register, MultiFunction Register, Up-Down Counter, Up-Down Counter: Testbench. Introduction to using FPGA Boards & Xilinx Tools.	5.6-5.11, 5.14
16	U 12/3	Data Path & Control Unit Partitioning, Data Path Design, Registers, Shift Registers, Modulo N (i.e. divide by N) Counters. Counters as Clock frequency dividers.	
17	T 14/3	Three-State Devices, A Register Bank with a 4-bit Data Bus, Design Steps. Digital System Design Example: Traffic Light Controller. **(Quiz#2)**	5.14-5.15
18	TH 16/3	Digital System Design Example: Traffic Light Controller. Algorithmic State Machine (ASM) Chart, Timing in ASM Charts. ASM Chart => Controller.	5.14-5.15
	TH 16/3	**Last Day for Dropping with W**	
19	U 19/3	ASM Chart => Controller, ASM Chart => Architecture/Data Processor, Implementing Controller, Algorithmic State Machine and DataPath (ASMD) Chart, ASMD Chart for 4-bit Counter. One's Count Circuit. Implementation of Data Path and Control Units of One's Count Circuit.	5.14-5.15
20	T 21/3	Design Examples: 2:1 Decimator, Scores Avg., Max. & Min., Counting Number of Elements ≥Target Value.	5.14-5.15
21	TH 23/3	Design Examples: Counting Number of Elements ≥Target Value.	5.14-5.15

	S 25/3	**Midterm Exam**	
22	U 26/3	Design Examples: Election Circuit. Solution of Midterm Exam.	5.14-5.15
23	T 28/3	Design Examples: Election Circuit, Transition Counting Circuit.	5.14-5.15
24	TH 30/3	Average of Serial Scores, Unsigned Divider.	5.14-5.15
	2-6/4	Midterm Vacation	
25	U 9/4	Behavioral Modeling of ASM, Linear Feedback Shift Register (LFSR), LFSR Modeling, Repetitive Algorithms: for loop.	5.9-5.11
26	T 11/4	FPGA Demo on using LCD screen.	
27	TH 13/4	**(Quiz#3)**	
28	U 16/4	Adder/Subtracter, Unsigned Division, Repetitive Algorithms: repeat loop, while loop, disable, forever. Tasks and Functions. Register File, Memory Unit.	5.11-5.13
29	T 18/4	File I/O system functions and tasks. Circuit Synthesis, Multilevel logic synthesis, Logic Network modeling.	5.14-5.16
30	TH 20/4	Network Optimization, Area and Delay estimation, Relation between testability and redundancy, Multilevel Logic Transformations: Elimination, Decomposition, Factoring.	6.1
	TH 20/4	**Last Day for Dropping all Courses with W**	
31	U 23/4	Multilevel Logic Transformations: Extraction, Simplification, Substitution, Fast Extraction. Synthesis & Testability.	6.1
32	T 25/4	Synthesis & Testability. Timing Issues in Multiple-Level Logic Optimization.	6.1
33	TH 27/4	Network Delay Modeling, topological critical path, false path, Algorithms for Delay Minimization.	6.1
34	S 29/4 (Sunday)	Behavioral or High-Level Synthesis: CDFG, scheduling, allocation. High-Level Synthesis Examples.	6.1
35	U 30/4	Synthesis of Combinational Logic. Synthesis of Priority Structures. Exploiting Logical Don't Care Conditions, Resource Sharing, Synthesis of Sequential Logic with Latches. Synthesis of Three-State Devices and Bus Interfaces, Synthesis of Sequential Logic with Flip-Flops.	6.1-6.6
36	T 2/5	Synthesis of Sequential Logic with Flip-Flops , Synthesis of Explicit State Machine. Exploiting Logical Don't Care Conditions**. (Quiz#4)**	6.1-6.6
37	TH 4/5	Synthesis of Gated Clocks and Clock Enable, Operator Grouping, Expression Substitution, Synthesis of loops.	6.1-6.6

38	U 7/5	Programmable Logic and Storage Devices: History of Computational Fabrics, ASIC vs. FPGA, FPGA Advantages, Reconfigurable Logic, Anti-Fuse-Based Approach.	Chapter 8
39	T 9/5	RAM Based Field Programmable Logic, Xilinx FPGA Families, The Xilinx 4000 CLB. LUT Mapping, Configuring the CLB as a RAM, FPGA Interconnect, Basic I/O Block Structure, CLB Structure, 5-Input Functions, Distributed RAM.	Chapter 8
40	TH 11/5	Distributed RAM., Shift Register, Carry & Control Logic. Adder Implementation, Carry Chain, 18 x 18 Embedded Multiplier. FPGA Design Flow – Mapping, Placement & Route. Memory Types, FPGA Memory Implementation, LUT-Based RAMS.	Chapter 8
41	U 14/5	Block RAM. Block RAM Logic Diagram, Block RAM Data Combinations and ADDR Locations, Read & Write Operations, Write Modes, Conflict Avoidance, Using Core Generator.	Chapter 8
42	T 16/5	**(Quiz#5)** Tutorial on using VGA and Ping Pong Game.	
43	TH 18/5	Tutorial on using VGA and Ping Pong Game.	
	TH 18/5	**Dropping all Courses with WP/WF**	