KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 405 Design and Modeling of Digital Systems

Term 122 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	S 26/1	Syllabus & Course Introduction. Introduction to Digital Design Methodology.	Chapter 1
2	M 28/1	Digital System Design Cycle, Architecture Design Example, Design Space and Evaluation Space, Digital System Complexity.	Chapter 1
3	W 30/1	Dealing with Design Complexity, Design Hierarchy, Abstractions, Design Domains & Levels of Abstraction, Design Methods, Design vs. Synthesis, Synthesis Process, Circuit Synthesis, Hardware Description Languages, Design Automation & CAD Tools, Design Flow in Verilog.	Chapter 1
4	S 2/2	Definitions: implicant, Prime Implicant, Essential Prime Implicant, Minimum cover, Minimal cover or irredundant cover. Shannon's Expansion, Boolean Expansion Based on Orthonormal Basis.	Chapter 2
5	M 4/2	Sum of Product (SOP) Simplification Procedure, Don't Care Conditions, SOP Simplification Procedure using Don't Cares, Product of Sum (POS) Simplification, Combinational Circuits Design Procedure.	Chapter 2
6	W 6/2	Combinational Circuits Design Procedure, Iterative Design, Decoders, Implementing Functions using Decoders.	Chapter 2
7	S 9/2	Multiplexers, Implementing Functions using Multiplexers. Sequential Circuit Model, Timing of Sequential Circuits, Latches and Flip-Flops, Sequential Circuit Design Procedure.	Chapter 2 & 3
8	M 11/2	Sequential Circuit Design Examples.	Chapter 3
9	W 13/2	Sequential Circuit Design Examples.	Chapter 3
10	S 16/2	State Minimization.	Chapter 3
11	M 18/2	State Minimization. **(Quiz#1)**	Chapter 3
12	W 20/2	Data Path & Control Unit Partitioning, Data Path Design, Registers, Shift Registers, Modulo N (i.e. divide by N) Counters.	

13	S 23/2	Three-State Devices, A Register Bank with a 4-bit Data Bus, Design Steps, Example: Traffic Light Controller.	
14	M 25/2	Communication between DP and CU: timing issues, Algorithmic State Machine (ASM) Chart, Timing in ASM Charts	5.14
15	W 27/2	ASM Chart => Controller, ASM Chart => Architecture/Data Processor, Implementing Controller, Algorithmic State Machine and DataPath (ASMD) Chart, ASMD Chart for 4-bit Counter.	5.14-5.15
16	S 2/3	2:1 Decimator, One's Count Circuit. Introduction, Why use HDL ?, Definition of a Module.	5.14-5.15, 4.1
17	M 4/3	Gate-level modeling, Verilog primitives, Verilog Syntax, Verilog Data Types, Module instantiation, Organization of a Testbench for Verifying a Unit Under Test (UUT).	4.1-4.2
18	W 6/3	Testbench Template, Propagation Delay, Inertial Delay, Transport Delay, Truth Table Models of Combinational and Sequential Logic with Verilog, Data Types for Behavioral Modeling.	4.2-4.4, 5.1-5.2
	W 6/3	**Last Day for Dropping with W**	
19	S 9/3	Boolean Equation-Based Behavioral Models of Combinational Logic, Assign Statement, Verilog Operators.	5.3
20	M 11/3	**(Quiz#2)**	
21	W 13/3	Propagation Delay & Continuous Assignment, Latches & Level-Sensitive Circuits, Always Block, Procedural Assignment	5.4-5.5
22	S 16/3	Wire vs. Reg, Algorithm-Based Models, if statement, case statement, D Latch, D Flip-flop (synchronous & asynchronous reset), Data Flow/ RTL Models: Shifter	5.6-5.8
23	M 18/3	Behavioral Models of Multiplexor, Encoder, Decoder, Seven Segment Display Decoder, Linear Feedback Shift Register (LFSR)	5.9-5.10
	T 19/3 (Makeup)	FPGA Tutorial	
24	W 20/3	No Class	
	23-27/3	**Midterm Vacation**	
25	S 30/3	LFSR Modeling, Repetitive Algorithms: for loop, repeat loop, while loop, disable, forever. Machines with Multicycle Operations. Tasks and Functions.	5.11-5.13
26	M 1/4	Tasks and Functions, Behavioral Modeling of Control Unit, Behavioral Models of Counters,	5.14-5.16

		Behavioral Models of Shift Registers.	
27	W 3/4		
	Th. 4/4	Midterm Exam	
28	S 6/4	Barrel Shifter, Universal Shift Register, Register Files. Circuit Synthesis, Multilevel logic synthesis. Solution of Midterm Exam.	5.16 & 6.1
29	M 8/4	Multilevel Logic Synthesis, Logic Network modeling, Network Optimization, Area and Delay estimation, Multilevel Logic Transformations: Elimination, Decomposition, Factoring, Extraction, Simplification, Substitution.	6.1
30	W 10/4	Timing Issues in Multiple-Level Logic Optimization: Network Delay Modeling, topological critical path, false path, Algorithms for Delay Minimization, Behavioral or High-Level Synthesis: CDFG, scheduling, allocation.	6.1
	W 10/4	**Last Day for Dropping all Courses with W**	
31	S 13/4	Synthesis of Combinational Logic, Synthesis of Priority Structures. Exploiting Logical Don't Care Conditions, Resource Sharing, Synthesis of Sequential Logic with Latches, Synthesis of Three-State Devices and Bus Interfaces, Synthesis of Sequential Logic with Flip-Flops.	6.2-6.6
32	M 15/4	**(Quiz#3)**	
33	W 17/4	Synthesis of Explicit State Machine	6.7
34	S 20/4	FPGA Tutorial#2 (LCD, Audio, ROM)	
35	M 22/4	Synthesis of Gated Clocks and Clock Enable, Operator Grouping, Expression Substitution, Synthesis of loops. Design and Synthesis of RISC Stored Program Machine (SPM).	6.11-6.13 & 7.3
36	W 24/4	Controller ASM Charts, RISC SPM Module, Processing Unit Module.	7.3
37	S 27/4	Processing Unit Module, Memory Module, Control Unit Module, RISC SPM Test Bench.	7.3
38	M 29/4	**(Quiz#4)**	
39	W 1/5	FPGA Tutorial#3: using Xilinx Core Generator.	
40	S 4/5	Universal Asynchronous Receiver Transmitter (UART), Block Diagram of a UART, UART Transmitter, UART Transmitter ASMD Chart, UART Transmitter Operation.	7.4
41	M 6/5	UART Transmitter Module, UART Transmitter ASMD Chart, UART Receiver, UART Receiver ASMD Chart, UART	7.4

		Receiver Module.	
42	W 8/5	Programmable Logic and Storage Devices: History of Computational Fabrics, ASIC vs. FPGA, FPGA Advantages, Reconfigurable Logic, Anti-Fuse-Based Approach, RAM Based Field Programmable Logic, Xilinx FPGA Families, The Xilinx 4000 CLB.	Chapter 8
	W 8/5	**Dropping all Courses with WP/WF**	
43	S 11/5	LUT Mapping, Configuring the CLB as a RAM, FPGA Interconnect, Basic I/O Block Structure, CLB Structure, 5-Input Functions, Distributed RAM, Shift Register, Carry & Control Logic, Adder Implementation, Carry Chain, 18 x 18 Embedded Multiplier.	Chapter 8
44	M 13/5	FPGA Design Flow – Mapping, Placement & Route, Memory Types, FPGA Memory Implementation, LUT-Based RAMS, Block RAM.	Chapter 8
45	W 15/5	Block RAM Logic Diagram, Block RAM Data Combinations and ADDR Locations, Read & Write Operations, Write Modes, Conflict Avoidance, Using Core Generator.	Chapter 8